

GR-81-6

CASS - A MICROCOMPUTER CONTROL SYSTEM FOR GRAND COULEE AGC SIGNALS

August 1981

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16. ABSTRACT <p>The CASS (Coulee AGC Signal Stuffer) is a microprocessor-based support control system to assist the large PMSC computers in the AGC control function at Grand Coulee Powerplant. The theory, operation, and program flow charts are presented.</p>			
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by

J. R. Schurz

T. R. Valdez



**Power and Instrumentation Branch
Division of Research
Engineering and Research Center
Denver, Colorado
August 1981**

UNITED STATES DEPARTMENT OF THE INTERIOR

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INTRODUCTION

In March 1979, it became apparent that the Grand Coulee PMSC (programmable master supervisory control) had timing problems which would result in poor AGC (automatic generation control). Under heavy processing of changing data within the plant, the total generated power may not be calculated as rapidly as required. This delay, which can range from 8 to 30 seconds, or more, will cause oscillation in the BPA (Bonneville Power Administration) control signals. The theoretical maximum delay around the loop is about 10 seconds before oscillation occurs.

At that time, the Power and Instrumentation Branch was requested to provide a processor that could substitute the total plant generation value sent from PMSC to BPA with a value derived from the presently used analog system. Construction of this processor, dubbed CASS (Coulee AGC signal stuffer), was begun in June 1980.

CONCLUSIONS

A processor was developed and installed at Grand Coulee in November 1980. This processor allows BPA to receive the actual plant total power generation with minimal delay, thus allowing BPA to implement AGC control of Grand Coulee.

As an added benefit, the installed processor derives and sends to PMSC a value for substitute generation. The operator is now relieved of the duty of manually entering changes in substitute generation.

The AGC control should be more predictable and stable as a result of this installation.

GENERAL DESCRIPTION

A block diagram of how CASS fits into the Grand Coulee PMSC system is shown in figure 1. The message sent from BPA Dittmer control center to Coulee PMSC, and vice versa, is intercepted by CASS. These messages are modified and then retransmitted. In the case of the message from PMSC to BPA, the total plant generation sent from the PMSC is replaced by the total plant generation as reflected by the analog chart recording system. This allows BPA to receive the total plant generation with minimal delay, the primary function of CASS.

In addition, CASS provides a secondary function to the operators of PMSC by intercepting and adding a quantity called substitute generation to the message from BPA to PMSC. This quantity is the total generation of Grand Coulee which is not under the control of PMSC. This quantity was previously entered by the operator into PMSC via a CRT (cathode ray tube) terminal. Figure 2 shows a block diagram of CASS. Within CASS is an integrator sensitive to any error between the total generation transmitted from PMSC and the total generation from the analog recording system. The output of this integrator is the derived value of substitute generation sent and automatically entered into PMSC, relieving the operator from doing so. The effect of this control loop is to force the total generation transmitted from PMSC to match that value measured by the analog recording system.

CASS has a front panel from which a number of quantities can be monitored, several of which can be outputted through D/A (digital-to-analog) converters for recording on strip charts. The front panel and its operation will be subsequently described.

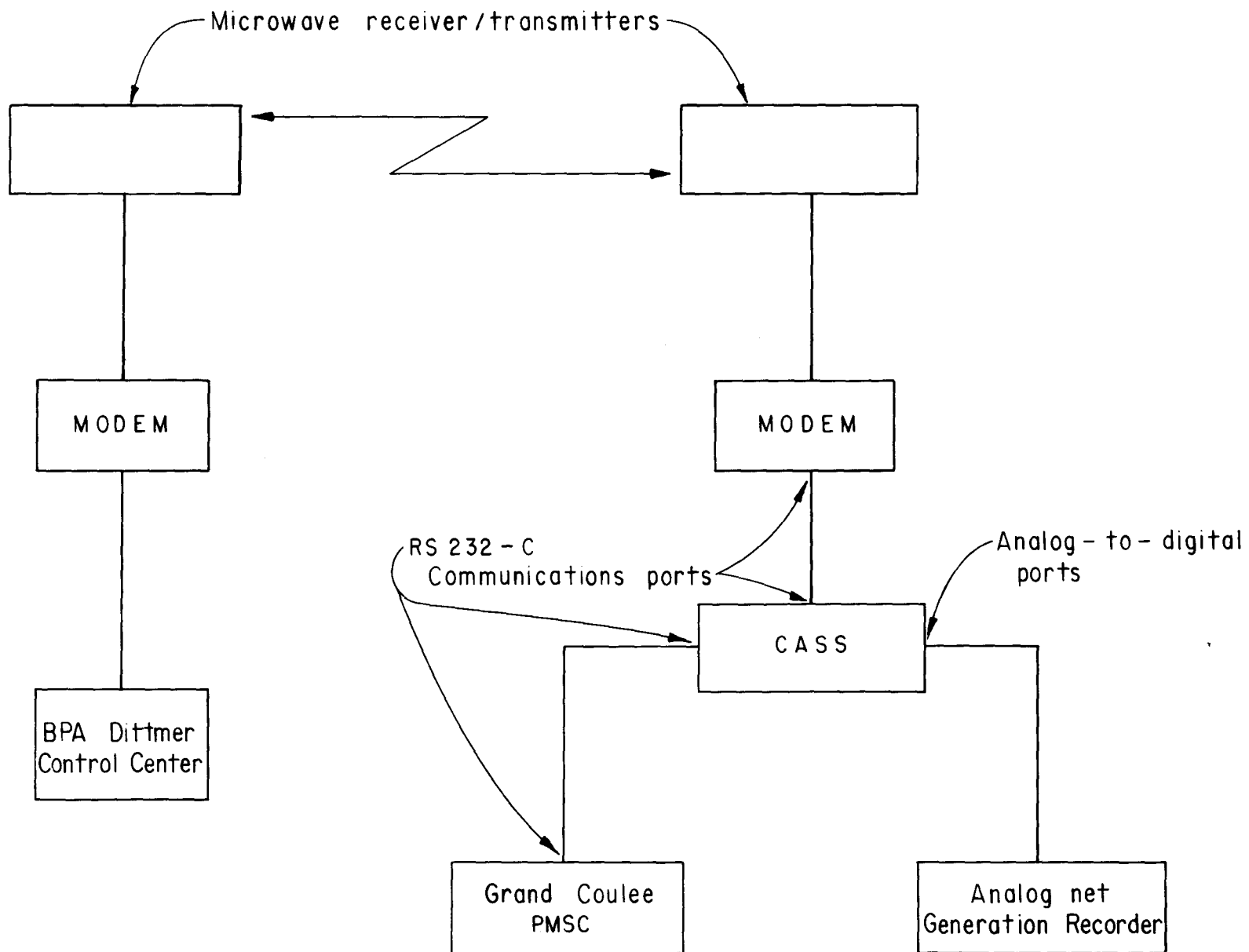


Figure 1.—Overview of communications system.

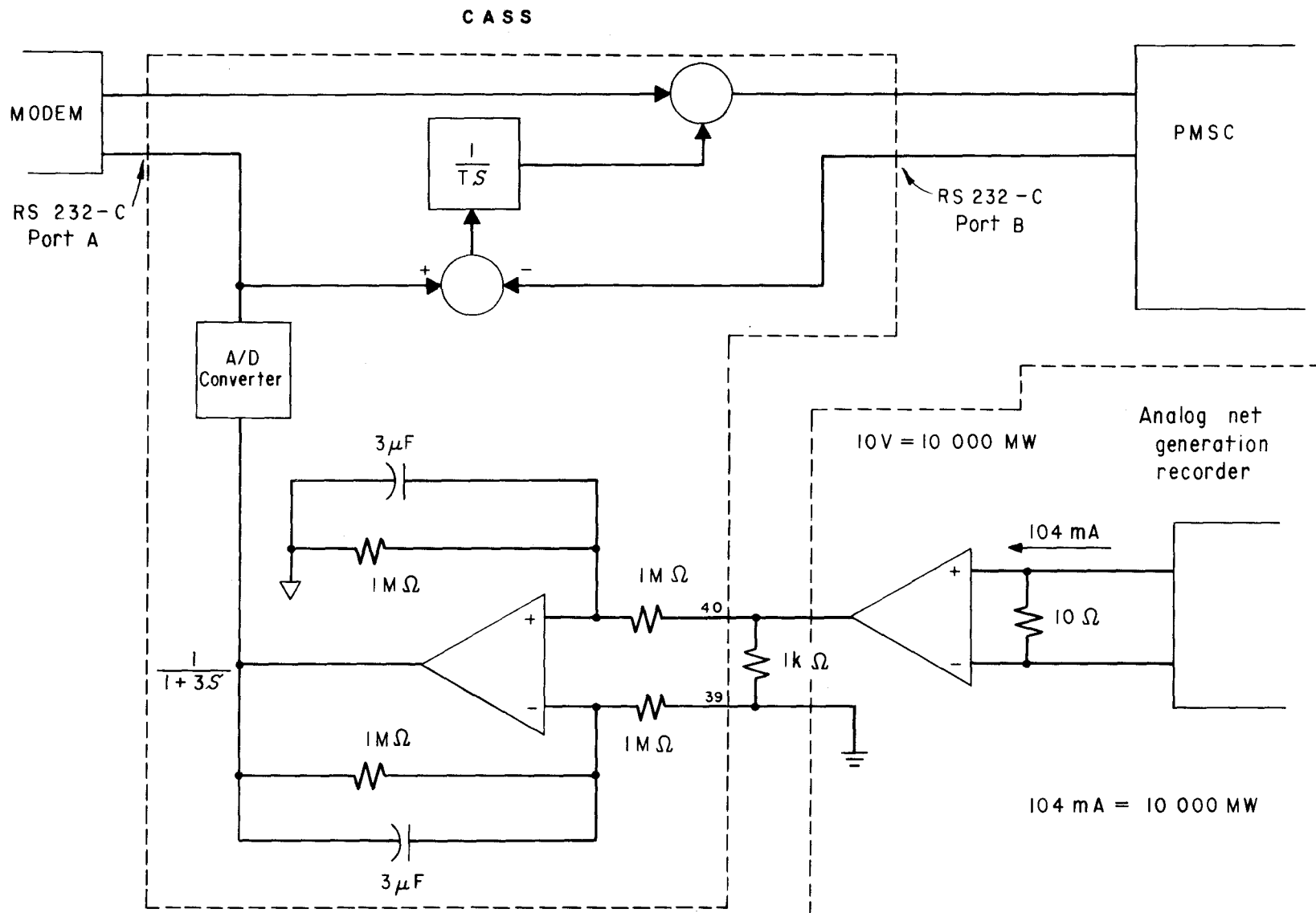


Figure 2.—Block diagram of CASS.

ANALOG AND DIGITAL MODELS

In order to verify the stability of the control loop associated with adding the integrator to derive substitute generation, a model of the system including CASS, PMSC, and BPA was tested on an analog computer. A block diagram of that model is shown in figure 3. The use of the analog computer provided a rapid means of showing the theory was valid, as well as providing step responses to compare with responses from digital models to verify their accuracy.

Subsequent to analog computer testing, the CASS software was developed along with digital models of BPA and PMSC. To test CASS, the digital models of BPA and PMSC were run on separate processors connected to CASS by RS232-C communications links. Step responses recorded on the digital model proved to be nearly identical to step responses recorded on the analog model.

HARDWARE DESCRIPTION

The CASS computer consists of five plug-in printed circuit cards described as follows:

1. A single-board, 16-bit microcomputer with vectored interrupts; one RS232-C compatible serial data port; two interval timers; a 16-bit parallel data port; 4096 words (4k) of ultraviolet-light-erasable, programmable read-only-memory (EPROM); and 512 words (0.5k) of random-access-memory (RAM).
2. A communication expansion card with four RS232-C compatible serial data ports and four interval timers.
3. An input-output expansion card with three 16-bit parallel data ports and three interval timers.

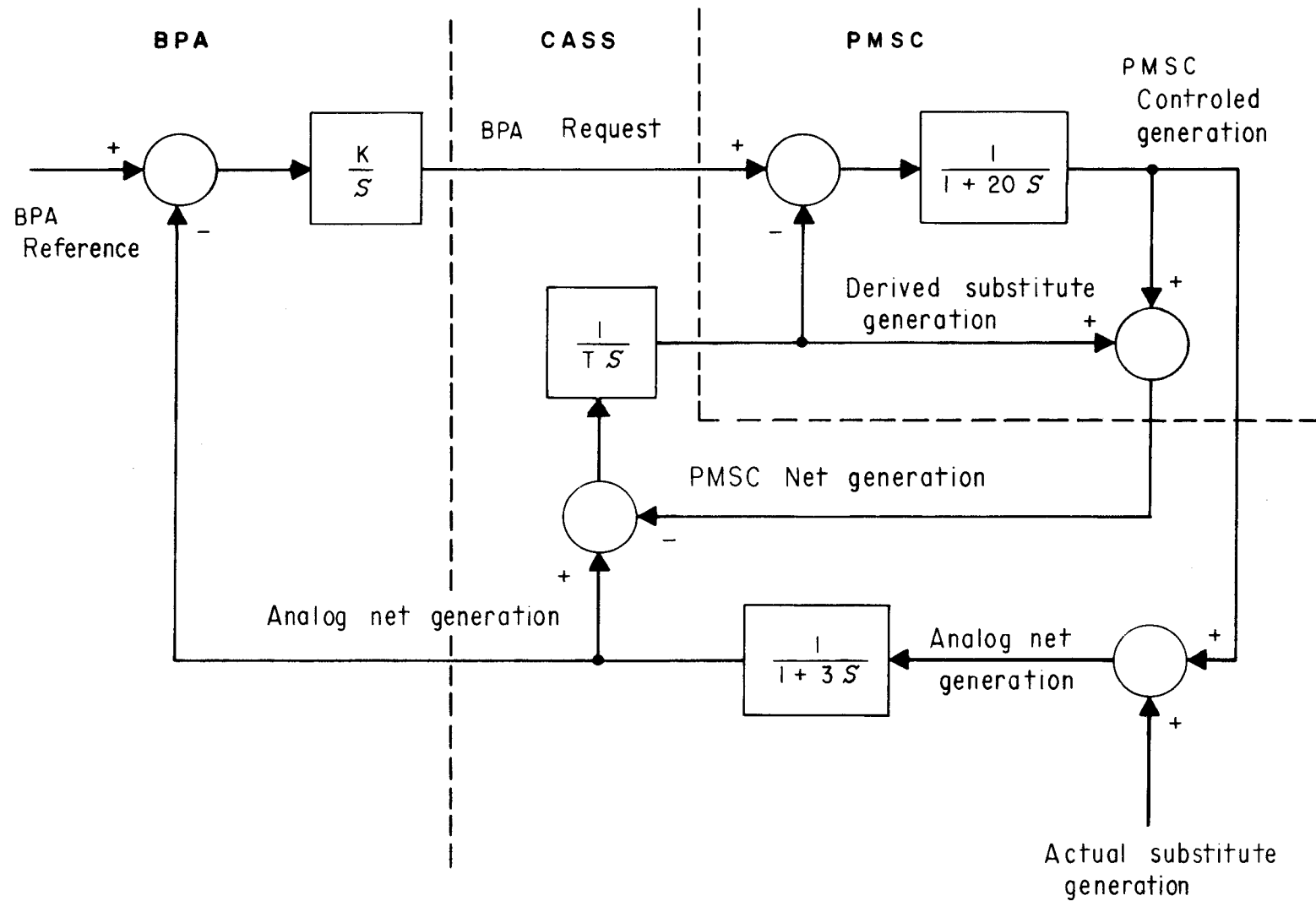


Figure 3.—Block diagram of system model.

4. An analog input-output card with 32 multiplexed, single-ended input channels and two analog output channels, each with 12 bits of resolution.

5. A prototyping board on which the Power and Instrumentation Branch built a differential input amplifier; three single-pole, double-throw switches; and five trimming potentiometers.

CASS has a front panel as shown in figure 4. This panel displays internal quantities, status, alarms, two D/A outputs, and two A/D (analog-to-digital) inputs.

SOFTWARE DESCRIPTION

The CASS software can be divided into five main routines. A brief description of each follows. The software is described more completely in the flow charts in appendix C and assembly language listings which are available upon request from the Power and Instrumentation Branch.

Communications

The software controlling the communications with BPA and PMSC uses two standard RS232-C serial data ports. These ports convert 7-bit parallel data to the standard 10-bit ASCII (American Standard Code for Information Interchange) serial format. This format consists of a 7-bit ASCII code representing the character to be transmitted, a parity bit, a start bit, and a stop bit. CASS uses even parity. The message structure consists of STX (start of text), up to 48 alphanumeric characters comprising the message, an ETX (end of text), a block check character, and an EOT (end of transmission).

8

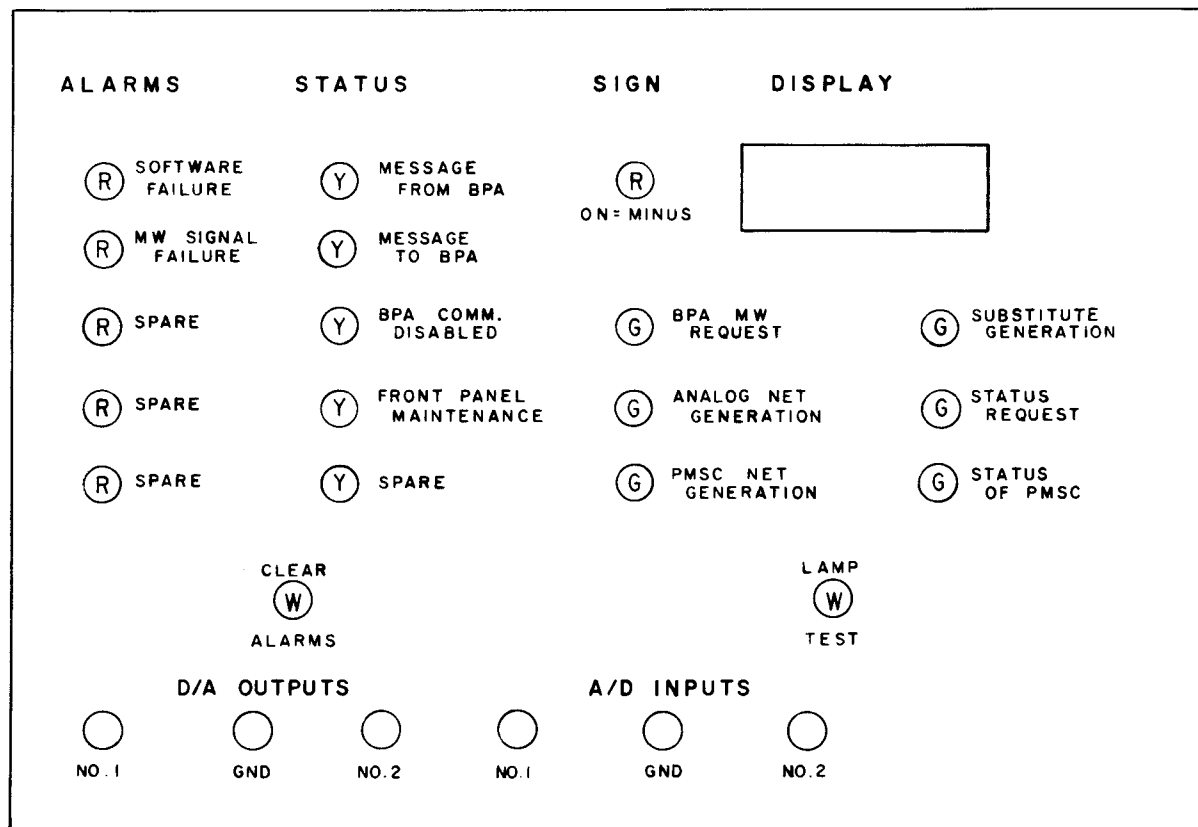


Figure 4.—Front panel.

A message is normally transmitted from BPA to PMSC every 2 seconds. This message is intercepted and received by the communications software which adds substitute generation to the message and initiates transmission to PMSC. When PMSC responds, this message is also intercepted and received by the communications software which removes the net generation calculated by PMSC and substitutes the net generation as measured by the analog recording system. This message is then transmitted to BPA.

If a transmission error is detected during receipt of a message, the checksum of the message, when retransmitted, will be set incorrectly, thus enabling BPA and PMSC to be aware of transmission errors. There are one flag and five error counters for each communications port. The flag and counters can be read from the front panel. See appendix A for address codes.

Analog-to-Digital and Digital-to-Analog

Another software routine controls the A/D and D/A conversions. The analog net generation signal from the analog recording system and the value of the five potentiometers are converted to digital values and stored in RAM. The routine also controls which of the four quantities will be outputted to the two D/A converters.

Front Panel

The front panel driver routine controls the display, all LED's (light-emitting diodes), and pushbuttons. The routine scans the pushbuttons for changes, provides debounce, decodes the address, and displays the appropriate quantity.

Integrator

The integrator routine derives the value of substitute generation. This routine is called every time a message is received from PMSC. The equation used for integration is:

$$\text{SUBGEN}_{\text{NEW}} = \text{SUBGEN}_{\text{OLD}} + \frac{(\text{ANALGEN} - \text{DIGGEN})}{(\text{INTEGRATION TIME})}$$

Because this equation assumes a sample interval of 1 second, the integration time must be scaled appropriately for different sample intervals. The sample interval is determined by the communications interval. For a communications interval of 2 seconds, integration time must be divided by two. This routine also reduces round off error by accumulating the remainder from the division.

Memory Maintenance

The fifth routine is memory maintenance. The software of this routing continually checks EPROM and RAM memory locations; if any location produces an error, the CPU enters an infinite loop. By using TIBUG, the type of error can be determined by examining "BADF" in the memory maintenance workspace. Details are given on the flow charts.

INSTALLATION AND OPERATION

To connect CASS into the system four connections are needed. They are:

1. 115 V, 60 Hz, a.c.
2. RS232 compatible connector carrying communications with BPA is connected to port A on the communications expander board.

3. RS232 compatible connector carrying communications with PMSC is connected to port B on the communications expander board.

4. A 40-pin edge connector with the output of the analog strip chart connected to pins 40 (plus) and 39 (minus) is connected to P-3 on the prototype board. This is a differential input. All switches on this board should be off (to the left) for the power-up.

Power is applied by the switch labeled "power" on the right side of the CASS chassis. Under normal circumstances, this should be all that is required for CASS to operate. Normal operation is signified by the left most red LED on the communications expander board blinking at 1 hertz and status LED's on the front panel, labeled "Message from BPA" and "Message to BPA", blinking at the communications rate.

The front panel, shown in figure 4, displays alarms, status, and interval quantities via the display and button selector. In addition, there are two channels of D/A output and two channels of A/D input (not used).

There are two alarm LED's, one of which is a "Software Failure" alarm. This alarm is activated and the computer enters an infinite loop when a checksum error occurs on a ROM sector or a RAM location fails to either set or clear properly. Location of the error can only be determined by using the TIBUG monitor routine described in appendix B. The alarm can be cleared by restarting the program with TIBUG, by operating the reset switch on the right of the CPU card, or with a power-down/power-up sequence.

The second alarm "MW Signal Failure" occurs when the power signal from the analog recording system is below 250 MW (+0.25 V) or above 9900 MW (+9.9 V). This alarm suspends all communications. Initially, the LED will flash; the alarm can be acknowledged by pressing the alarm clear button, then the LED will remain on. When the problem has been corrected, pushing the alarm clear button will turn the LED off and enable communications.

There are four status LED's. The one labeled "Message from BPA" indicates a message has been received from BPA and transmitted to PMSC. A STX received from BPA enables the LED. Therefore, the LED should flash for each message being received from BPA and transmitted to PMSC. The status LED labeled "Message to BPA" provides the same function as the previously described LED but for transmission from PMSC to BPA.

The third LED labeled "BPA Communications Disabled" is an indication that S1 on the protoboard has been turned on. The fourth LED labeled "Front Panel Maintenance" is an indication that S3 on the protoboard has been turned on. The function of these switches will be subsequently described.

The front panel has a four-digit display with an LED to indicate polarity. This display will indicate those values requested by pushing one of the six pushbuttons below the display. These six quantities are: (1) the setpoint, in megawatts, for Grand Coulee being requested by BPA, (2) the total generation, in megawatts, of Grand Coulee as recorded by the analog recording system, (3) the total generation, in megawatts, of Grand Coulee as measured by the PMSC, (4) the substitute generation, in megawatts, being derived and sent to PMSC by CASS, (5) the plant status requested by BPA (-1 = auto or base load; 0 = standby or off), and (6) the plant status of the PMSC (-1 = auto, 0 = off). The quantity being displayed is indicated by an LED within the pushbutton which selects that quantity.

There are two D/A outputs available on the front panel. The scaling for both outputs is 10 V = 10 000 MW. D/A No. 1 provides an analog output of the substitute generation derived by CASS with an option for an analog output of the total generation of Grand Coulee as totaled by the analog recording system. D/A No. 2 provides an analog output of the total generation as totaled by the PMSC with an option for an analog output of the setpoint requested by BPA. Exercising the options is described in appendix A. There are two A/D channels available but not used.

The lamp test button will light all LED's and all segments and decimal points in the display.

There is a program in ROM that will test the display on the front panel. This program will repeatedly increment each digit from 0 through 9 and flash the decimal points. This program must be run from TIBUG. To start, set the PC (program counter) to 16010 octal and the ST (status) register to zero, then press the letter E (execute). To return to TIBUG, use either the reset button on the CPU or the halt switch on the chassis.

For other than normal operation of CASS, there are three switches located on the prototype board. All switches should be off for normal operation. Switch S1, labled "BPA Communication Disabled", when turned on allows communications between CASS and PMSC only. This operating mode is to provide automatic substitute generation updating to PMSC when communications with BPA have been lost and are anticipated to be lost for a considerable length of time. The message transmitted from CASS to PMSC will request a plant status of "off" and a BPA request of no power. In this mode, the first two status lights will alternately flash as messages are transmitted and received. This substitute message is transmitted at an interval set by R4. In order to maintain the same integration gain in CASS while in this mode, the communications interval should be the same as that from BPA. Upon restoration of communications with BPA, switch S1 must be returned to the "off" position in order to enable the BPA communication interrupts.

Switch S2, labled "Power-up Vector", when turned on forces CASS to power-up into the TIBUG monitor routine instead of the main program. This debug routine allows one to examine and change registers, examine and change RAM memory locations, manipulate input and output lines, set breakpoints, single step through programs, and execute programs. The routine is described in appendix B.

Switch S3, labled "Front Panel Maintenance", when turned on, puts the front panel in the maintenance mode. In this mode, the six pushbuttons on the front panel can be used to address 1 of 77 octal locations for display. The least significant digit is the right row of

three buttons with the top button being the least significant bit. Any button pushed will light if unlit or extinguish if lit. Those buttons lit indicate the octal code for the quantity being displayed. Appendix A lists the quantities that can be displayed and their octal address codes.

There are five trimming potentiometers located on the prototype board. The first four are used; the last is a spare. Potentiometer R1 is used to set the integration time on the integrator within CASS which derives substitute generation. This value is displayed on the front panel by using octal address 11. This integration time is the quantity displayed times the communications interval in seconds. Thus, with a display of 25 and a communication interval of 2 seconds, the integration time is 50 seconds resulting in an integration gain of 0.02. This potentiometer has a range of 0 to 199 on the display.

Trimming potentiometer R2 sets a timer with a range of 0 to 19 seconds and an octal address of 12. Upon power-up, CASS attempts to set substitute generation to approximately the right value. This is accomplished by initially setting substitute generation to zero on the messages being sent to PMSC. After the first message is received from PMSC, the timer set by R2 begins to time out. At the end of the time interval, the total generation from BPA is subtracted from the total generation as measured by the analog recording system. The result approximates the value of substitute generation. This timer should be set for the minimum amount of time necessary for PMSC to call the AGC algorithm after receiving the substitute generation value of zero.

Trimming potentiometer R3 is a calibration adjustment for the total generation measured by the analog recording system. This value is addressed by octal code 13 and has a range of -10.0 to $+9.9$ percent.

Trimming potentiometer R4 sets the communications interval for the substitute message being transmitted by CASS to PMSC (S1 on) when BPA communications is disabled. The potentiometer has a range of 0.0 to 19.9 seconds and is addressed by octal code 14. The time interval should be set the same as the communications interval from BPA.

FIELD TESTS

In November 1980, CASS was installed in the PMSC computer room in the 480-mm (19-in) rack containing the primary communications preprocessor. Testing revealed two minor software problems in the PMSC master. The first problem prevented the status bit in the message from PMSC to BPA from indicating "auto" when the PMSC was in the "BPA" mode. The second problem related to declaring the AGC communications port down on the PMSC; declaring this port down opens the control loop between CASS and PMSC because the master no longer provides current data to the communication preprocessor. This control loop derives substitute generation. With the port declared down, the communications preprocessor continues to respond to messages from CASS, returning data that are no longer current. This causes the integrator within CASS which derives substitute generation to continually integrate. This will be corrected by a software change in the PMSC master which will, when the AGC port is declared down, instruct the communications preprocessor not to respond to messages from CASS. This will maintain the derived value of substitute generation at the value it was prior to declaring the port down.

Because the BPA computer system was not ready for AGC tests, we were unable to test the AGC mode with BPA, although communications were tested and found to operate correctly. AGC testing was then accomplished by using another processor to simulate BPA. Some results from these tests are shown in figures 5 through 8. These figures show a step change of 40 MW in the reference on the BPA model. The integration time in the BPA model and CASS is 20 and 50 seconds, respectively. The left side of figure 3 shows the model used for BPA.

The top trace of figure 5 shows the total generation as measured by the analog system and read by CASS. This total generation value for Grand Coulee is being sent to BPA in lieu of the value measured by the PMSC system. Figure 6 shows the total generation as measured by PMSC. This is the quantity that can be as much as 28 seconds behind real time under heavy processing of changing data within the plant. At this time, the delay is

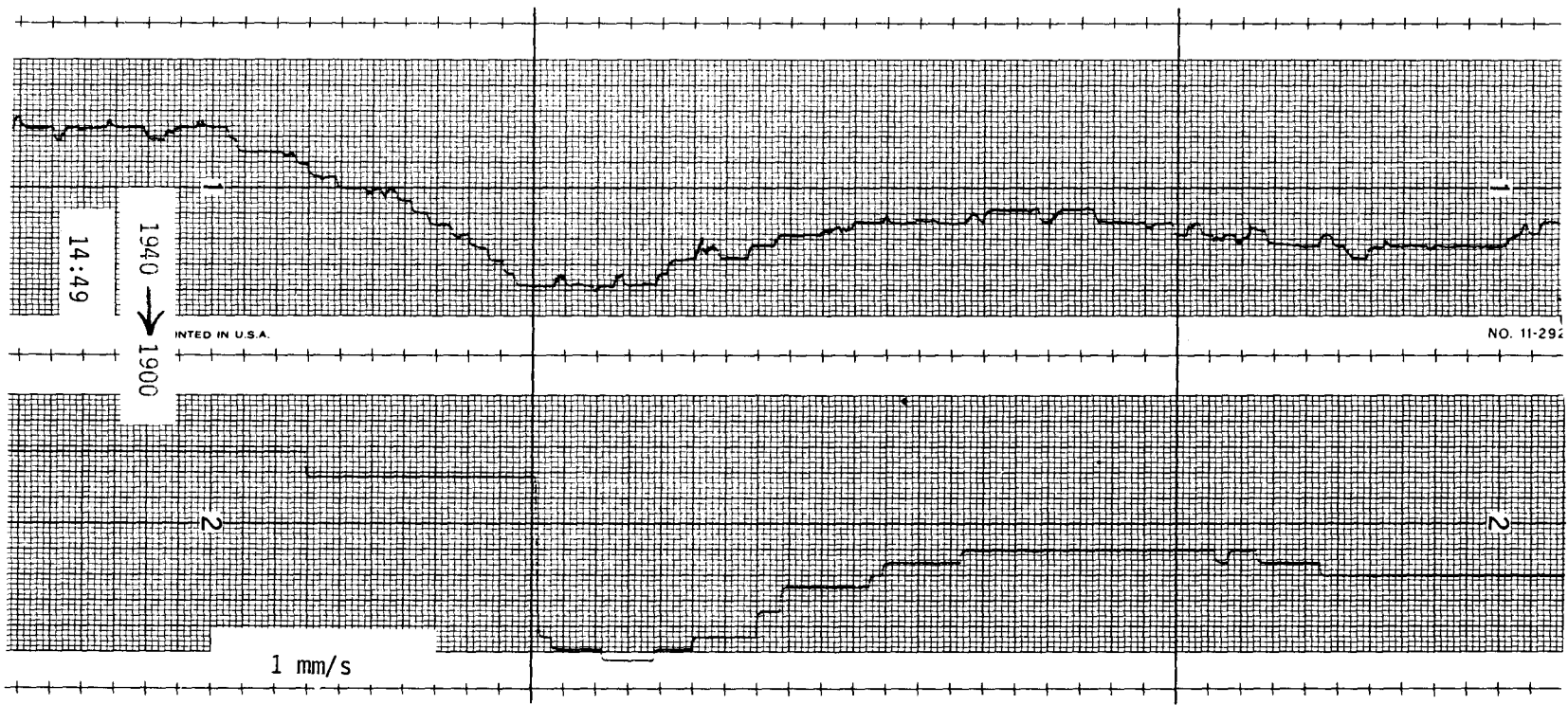


Figure 5.—Comparison of analog and PMSC plant totals, case I.

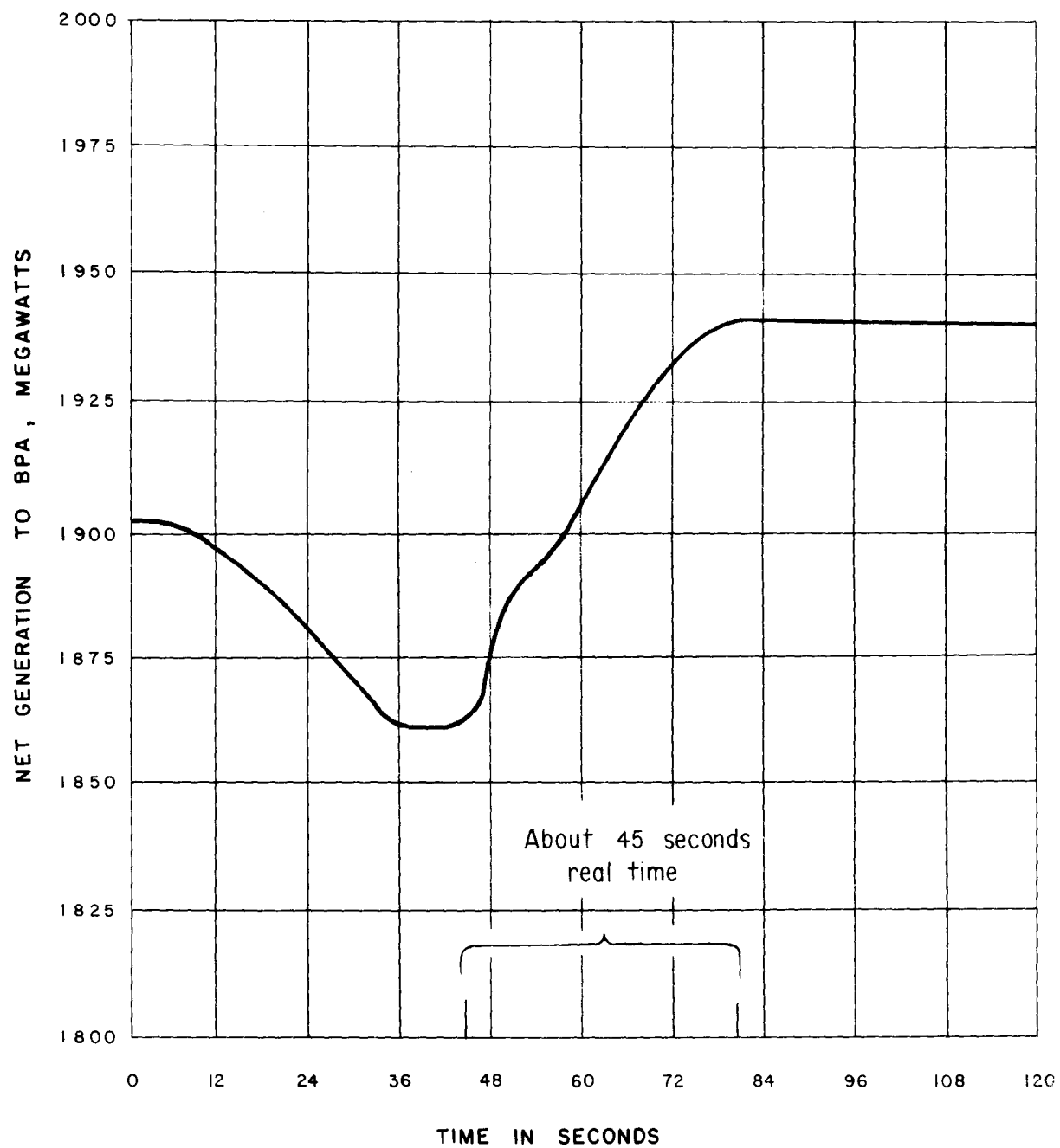
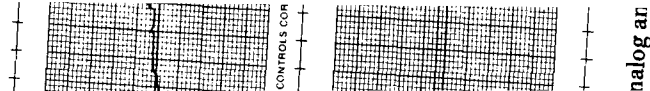


Figure 6.—Total generation as measured by PMSC, case I.



not evident as the master is communicating with only a small number of RTU's (remote terminal units). The upper trace of figure 5 and figure 6 compare very well, except for the time axis on figure 6. This axis is based on the PMSC master calling the AGC routine every 2 seconds, when in fact, the time varies considerably and averaged, under the lightly loaded conditions, about 2.5 seconds.

The lower trace of figure 5 shows the total generation as measured by the PMSC (fig. 2) after being transferred to the communications preprocessor and then transmitted to CASS. The interesting point of this record is the appearance of a previously unknown system hangup between the PMSC master and the communications preprocessor of about 35 seconds during which current data were not being transferred from the master to the preprocessor. This time delay was observed in five of six records and ranged from 15 to 40 seconds. Because CASS does not send this value to BPA but uses it only to derive substitute generation, there will be very little effect on the AGC control loop as long as the CASS integrator time is large, at least 50 seconds. This problem is being investigated.

Figures 7 and 8 show the same quantities as figures 5 and 6, but in this case, there does not appear to be a system hangup. The change is relatively stable with about 30 percent overshoot on the first swing. Recovery to within 10 percent of the setpoint occurs in less than 3.5 minutes. These values result from an integration time of 20 seconds in the BPA model. In reality, the integration time of BPA is probably larger which will result in more stable operations.

The control loop deriving substitute generation, although purposely set slow so as not to affect the PMSC AGC mode, was a beneficial addition to CASS. The operators are now relieved of periodically entering changes in the generation quantities not being measured by the PMSC.

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APPENDIX A

Descriptions of Interval Variables and Corresponding Octal Address Codes

Octal Code	Description
01	Substitute generation (megawatts)
02	Status requested by BPA (- 1 = Auto or Base, 0 = Standby or Off)
03	Front panel A/D No. 1
04	Status of PMSC (- 1 = Auto, 0 = Off)
05	Front panel A/D No. 2
06	Spare
07	Spare
10	BPA request (megawatts)
11	Potentiometer No. 1 Integration rate (Must be multiplied by communications interval to obtain integration time)
12	Potentiometer No. 2 Integrator reset time (0 to 19 seconds)
13	Potentiometer No. 3 Analog calibration (- 10.0 to + 9.9 percent)
14	Potentiometer No. 4 Communications time interval (0.0 to 19.9 seconds)
15	Potentiometer No. 5 Spare
16	Spare
17	Spare
20	Total generation measured by analog recording system (megawatts)
21-37	Spares
40	Total generation measured by PMSC (megawatts)
41-47	Spares

APPENDIX A

Descriptions of Interval Variables and Corresponding Octal Address Codes

— Continued

Octal Code	Description	
50	BPA communications error flag (A minus 1 indicates there was an error in the last message)	
51	BPA checksum error counter	} Detected by the communications controller TMS 9902
52	BPA parity error counter	
53	BPA framing error counter	
54	BPA overrun error counter	
55	BPA receive buffer overrun error counter	
56	Spare	
57	Spare	
60	PMSC communications error flag (A minus 1 indicates there was an error in the last message)	
61	PMSC checksum error counter	} Detected by the communications controller TMS 9902
62	PMSC parity error counter	
63	PMSC framing error counter	
64	PMSC overrun error counter	
65	PMSC receive buffer overrun error counter	
66-67	Spares	
	All locations above 70 (octal) can be flags that are toggled from 0 to -1, when selected, by the lamp test button.	
70	Spare	
71	Selects the output for D/A No. 1 (0 = Substitute generation; -1 = Total generation from analog recording system)	
72	Selects the output for D/A No. 2 (0 = Total generation from PMSC; -1 = BPA request)	
73-77	Spares	

APPENDIX B

Description of TIBUG

The TIBUG is a debug monitor which provides an interactive interface between the user and the CPU. This monitor was supplied by TI (Texas Instruments) with the 990/100M CPU boards and subsequently modified by the Power and Instrumentation Branch to better suit our needs.

Communication with TIBUG is through the RS232-C port on the CPU board at a baud rate of 2400.

The TIBUG commands are listed in table B1. The original **D** and **A** commands have been deleted, the function of the **T** command changed, and the **G** command added to TI's original version. Further information on TI's TIBUG and detailed descriptions of the commands are available in TI publication "TM 900/100M Microcomputer User's Guide."

Table B1

T - TABLE

Table Pointer = WP	PC	ST						
WP = R0	R1	R2	R3	R4	R5	R6	R7	
R8	R9	R10	R11	R12	R13	R14	R15	
PC - 10B = I	I	I	I	Next I	I	I	I	
		↓	↓	Branch	↓	↓		
		C	C	Address	C	C		
Memory Address = C	C + 2	C + 4	C + 6	C + 10	C + 12	C + 14	C + 16	
	C + 20	C + 22	C + 24	C + 26	C + 30	C + 32	C + 34	C + 36

EXECUTERS - Use restart and/or halt to get out of last breakpoints.

B <address> <CR>	Sets breakpoint at address and executes.
G <address> <CR>	Single steps to breakpoint (used for breakpoints within ROM)
S	Single steps from present PC
E	Execute beginning at present WP and PC

Examine/Change

M <add 1>, <add 2> <CR>	List memory from address 1 to address 2
M <address> <CR>	Opens memory location

M <CR>	Opens last memory location
<space>	Increments through memory
<minus>	Decrements through memory
C <base address>, <number of bits> <CR>	CRU examine
W <register number> <CR>	Opens appropriate register
W <CR>	Opens last register
<space>	Increments through registers
<minus>	Decrements through registers
R	Opens WP
<space>	Increments to PC and ST
<minus>	Displays the present position again
L	Load from right magnetic tape on an HP 2645A terminal.
F <add 1>, <add 2>, <pattern>, <CR>	Finds and lists all locations, with the particular pattern between address 1 and address 2.

Abbreviations and symbols used in table B1

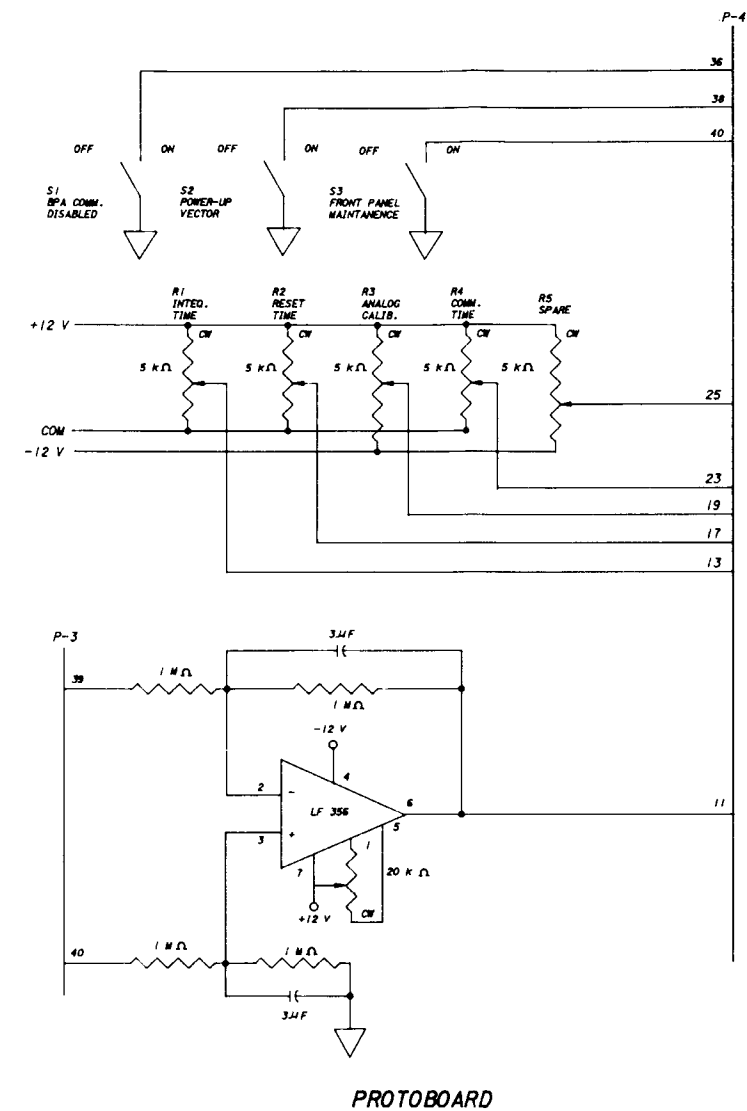
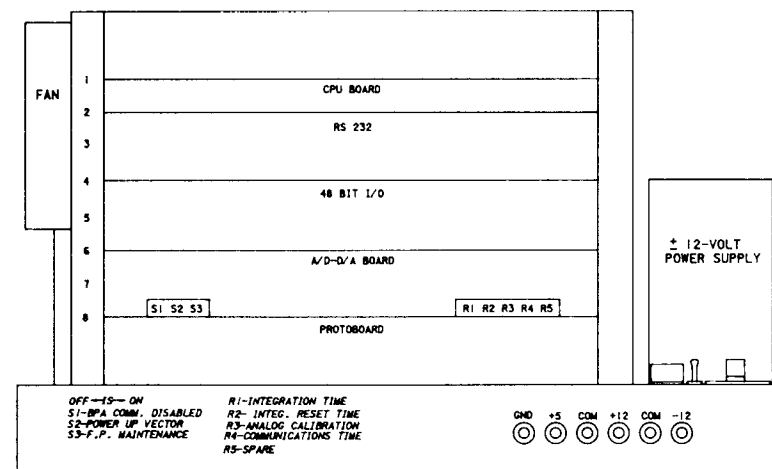
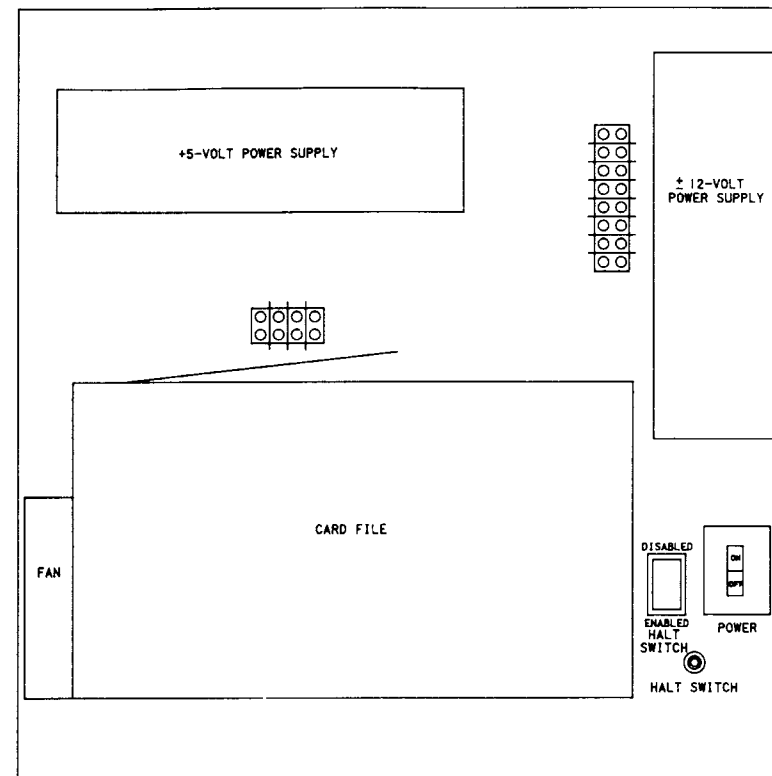
< > Items within the brackets are supplied by the user. All addresses, registers, and contents must be in octal.

I	Instruction
C	Contents
WP	Workspace pointer
PC	Program counter pointer
ST	Status register
CR	Carriage return
CRU	Communica- tions register unit

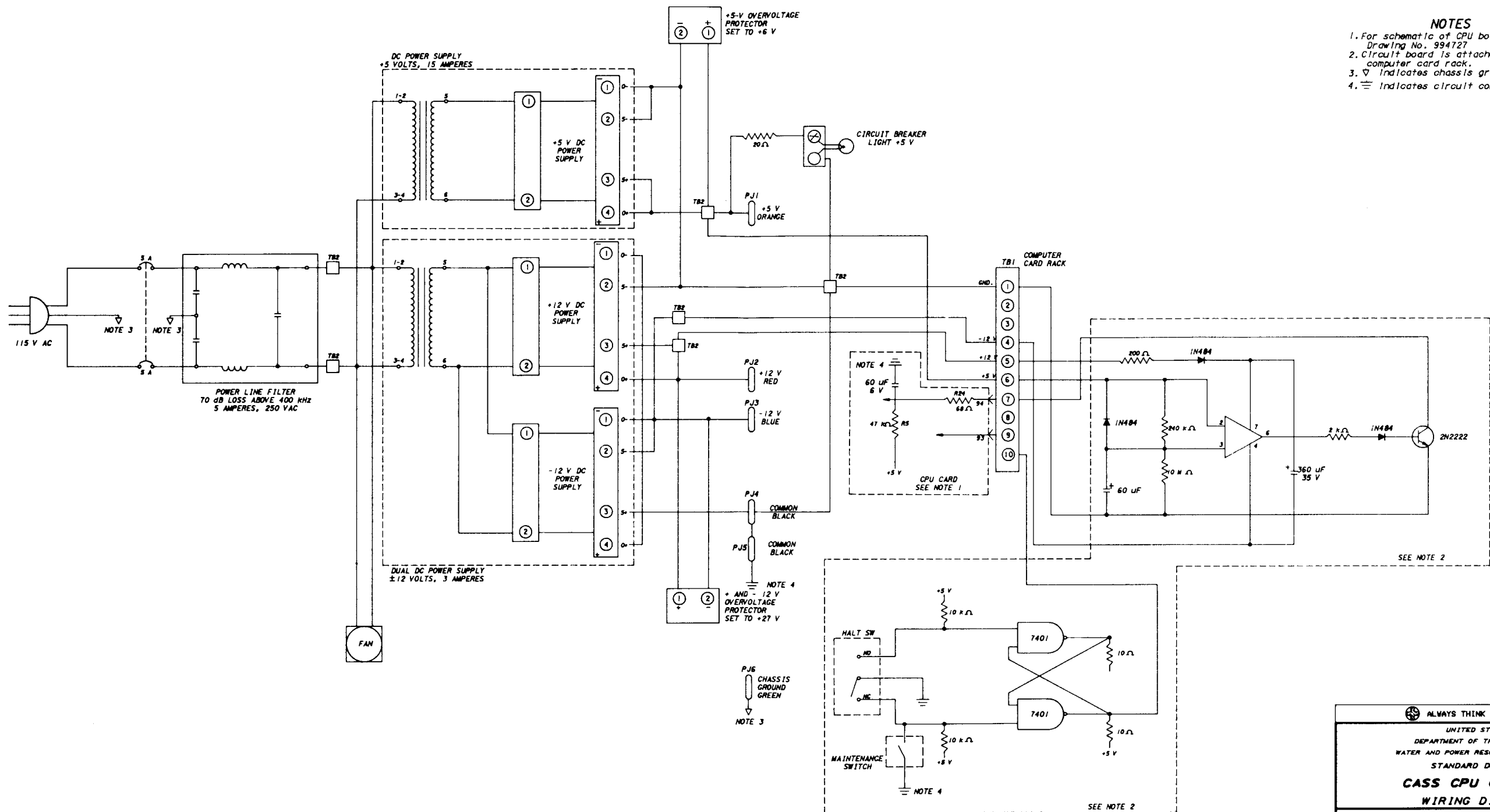
APPENDIX C

Drawings and Flow Charts

<i>Drawings</i>	<i>Number</i>
Chassis layout and protoboard	100-PI-001
CPU chassis wiring diagram	100-PI-002
Card file wiring	100-PI-003
Front panel layout and wiring	100-PI-004
 <i>Flow Charts</i>	
Executive	100-PI-005
A/D and D/A converter and calibration	100-PI-006
Front panel driver, sheet 1	100-PI-007
Front panel driver, sheet 2	100-PI-008
Display driver	100-PI-009
BPA communications interrupt	100-PI-010
BPA communications formatter	100-PI-011
PMSC communications interrupt	100-PI-012
PMSC communications formatter	100-PI-013
Integrator	100-PI-014
Memory maintenance	100-PI-015
Scale XOP 0	100-PI-016
ASCII to binary XOP 1, binary to ASCII XOP 2	100-PI-017



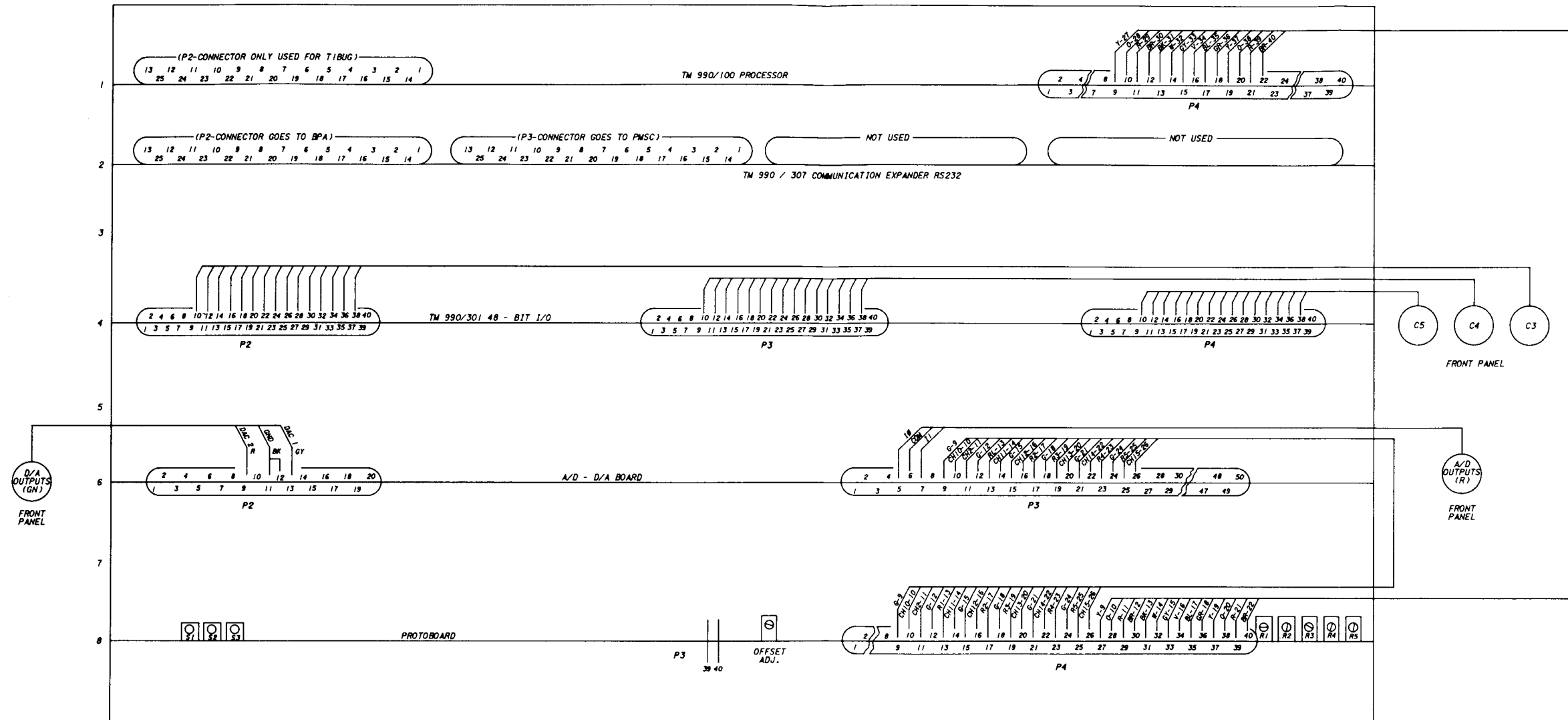
ALWAYS THINK SAFETY	
UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS	
CASS CHASSIS LAYOUT & PROTOBOARD	
DESIGNED.....	TECHNICAL APPROVAL.....
DRAWN.....	C.W. OPIC SUBMITTED.....
CHECKED.....	APPROVED.....
DENVER, COLORADO	JAN. 1, 1981
100-PI-001	



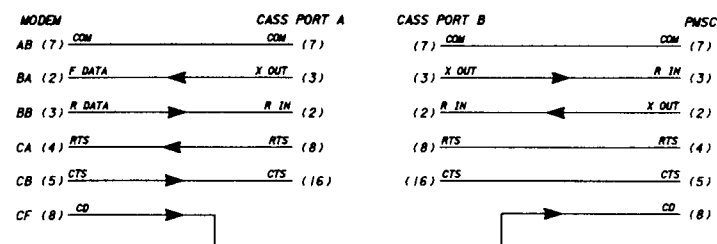
- NOTES**
1. For schematic of CPU board see T1 Drawing No. 994727
 2. Circuit board is attached to back of computer card rack.
 3. ▽ indicates chassis ground.
 4. ≡ indicates circuit common.

NOTE 1
Circuit board is attached to back of computer card rack.

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UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS	
CASS CPU CHASSIS WIRING DIAGRAM	
DESIGNED BY D.B. DRULLMANN	TECHNICAL APPROVAL SUBMITTED
CHECKED BY J.V.	APPROVED
DENVER, COLORADO	JAN. 1, 1981
100-P1-002	



COMMUNICATIONS CABLES

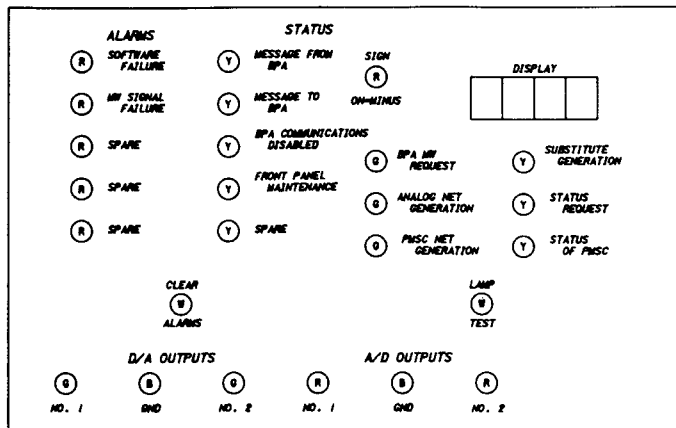


PROTOBOARD TABLES

S1-BPA COMM. DISABLED
S2-POWER-UP VECTOR
S3-FRONT PANEL MAINTENANCE
P3-39 } ANALOG SIGNAL INPUT
P3-40 }

R1-INTEGRATION TIME
R2-INTEGRATION RESET TIME
R3-ANALOG CALIBRATION
R4-COMMUNICATION TIME
R5-SPARE

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<p>DESIGNED _____</p> <p>DRAWN D.E. BINGAMAN</p> <p>CHECKED T.V.</p>	<p>TECHNICAL APPROVAL _____</p> <p>SUBMITTED _____</p> <p>APPROVED _____</p>
<p>DENVER, COLORADO</p>	<p>JAN. 1, 1981</p> <p>CHIEF, ELECTRICAL BRANCH</p> <p>100-PI-003</p>



WIRING DIAGRAM
REAR VIEW

Least significant digit of display

* Pins F & D of the displays shall be wired as follows:

DIGIT 4 PIN F
DIGIT 4 PIN D
DIGIT 3 PIN F
DIGIT 3 PIN D

P2 (PIN 3)
CABLE C3

DIGIT 2 PIN F
DIGIT 2 PIN D
DIGIT 1 PIN F
DIGIT 1 PIN D

P3 (PIN 3)
CABLE C3

All other +5 V & GND points shall be wired to terminal block TBI.

Terminal block mounted on back of door. Mounted screw heads toward front.

Black banana jack for connection to CPU chassis ground front jack

Red banana jack for connection to CPU chassis +5 V front jack

These cables go to the A/D card (slot 3) see 245-EP-1004

CONNECTOR PIN NO.	CABLE DESIGNATION	DEVICE	CRU BASE (B)
P0	P2-20	D4B0	DEC
P1	22	D4B1	1
P2	14	D4B2	2
P3	16	D4B3	4
P4	18	D4B4	8
P5	10	D4B5	BLNK
P6	12	D3B0	DEC
P7	24	D3B1	1
P8	26	D3B2	2
P9	28	D3B3	4
P10	30	D3B4	8
P11	32	D3B5	BLNK
P12	34	D2B0	DEC
P13	36	D2B1	1
P14	38	D2B2	2
P15	40	D2B3	4

To 48-bit I/O card P2 connector
CABLE C3

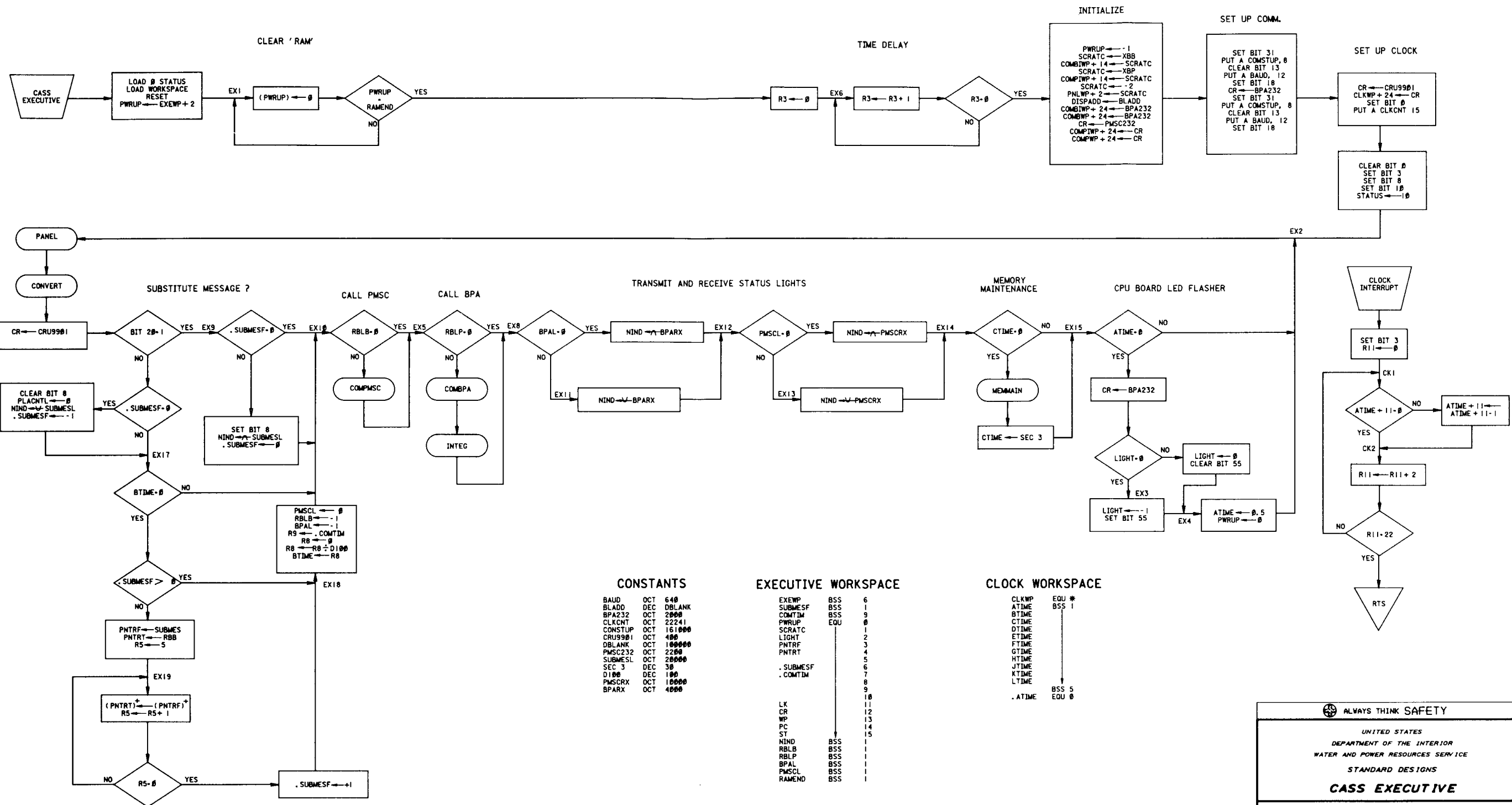
P0	P3-24	D2B4	8
P1	22	D2B5	BLNK
P2	14	D1B0	DEC
P3	16	D1B1	1
P4	18	D1B2	2
P5	10	D1B3	4
P6	12	D1B4	8
P7	24	D1B5	BLNK
P8	26	SIGN	SIGN LED
P9	28	SUBGENB	DISPLAY SELECTORS (BUTTONS)
P10	30	BPASTAB	DISPLAY SELECTORS (BUTTONS)
P11	32	PMSCSTAB	DISPLAY SELECTORS (BUTTONS)
P12	34	BPASETb	DISPLAY SELECTORS (BUTTONS)
P13	36	ANALGENB	DISPLAY SELECTORS (BUTTONS)
P14	38	PMSCGENB	DISPLAY SELECTORS (BUTTONS)
P15	40	SUBGENL	DISPLAY SELECTORS (BUTTONS)

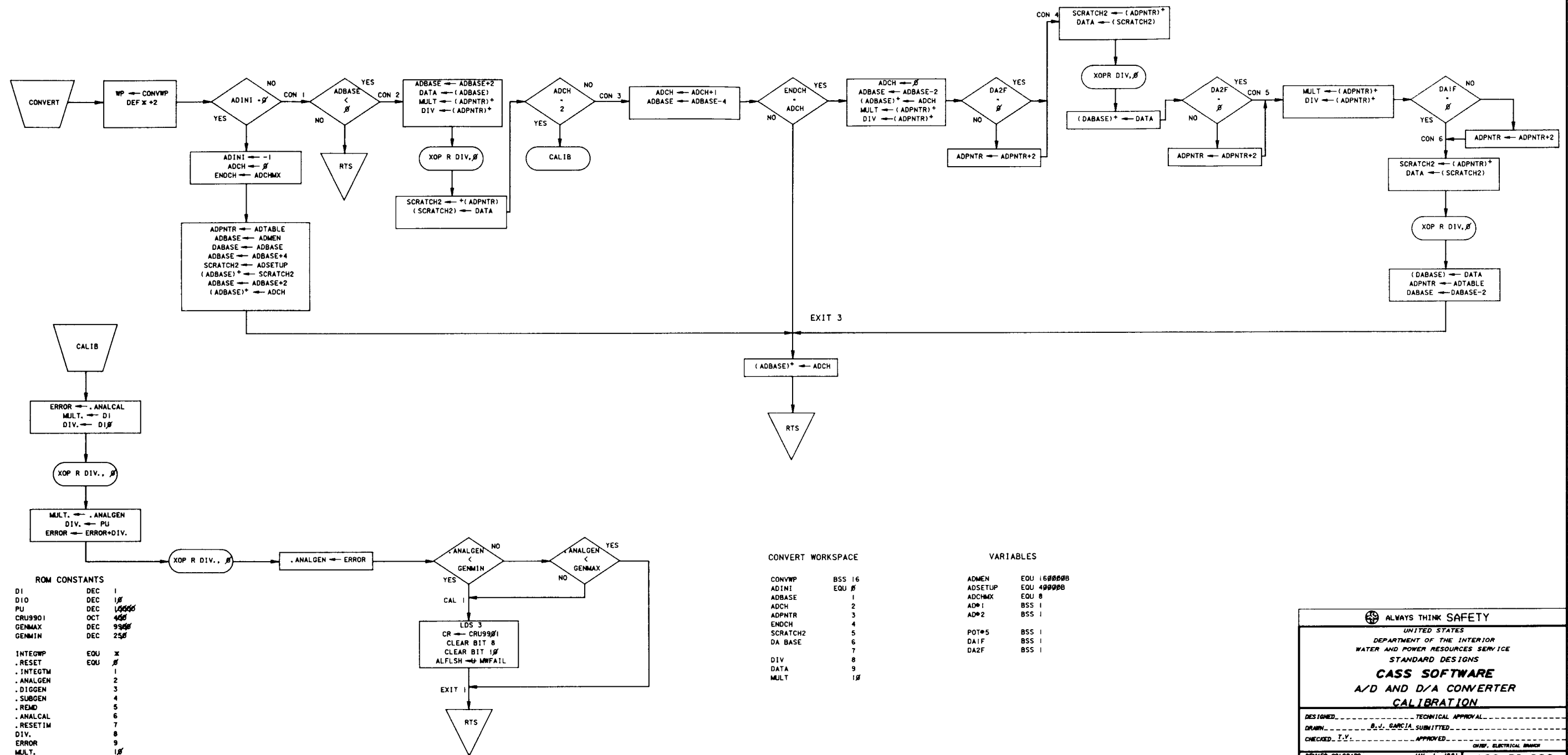
To 48-bit I/O card P3 connector
CABLE C4

P0	P4-20	BPASTAL	DISPLAY SELECTOR LED'S
P1	22	PMSCSTAL	DISPLAY SELECTOR LED'S
P2	14	BPASETl	DISPLAY SELECTOR LED'S
P3	16	ANALGENL	DISPLAY SELECTOR LED'S
P4	18	PMSCGENL	DISPLAY SELECTOR LED'S
P5	10	AL1	ALARM LED'S
P6	12	AL2	ALARM LED'S
P7	24	AL3	ALARM LED'S
P8	26	AL4	ALARM LED'S
P9	28	AL5	ALARM LED'S
P10	30	STAT1	STATUS LED'S
P11	32	STAT2	STATUS LED'S
P12	34	STAT3	STATUS LED'S
P13	36	STAT4	STATUS LED'S
P14	38	TESTB	LAMP TEST BUTTON
P15	40	CLRb	CLEAR ALARMS BUTTON

To 48-bit I/O card P4 connector
CABLE C5

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DESIGNED: T.V.	TECHNICAL APPROVAL: C.W. OPIE
CHECKED: T.V.	SUBMITTED: APPROVED:
<p>DENVER, COLORADO</p> <p>JAN. 1, 1981</p> <p>100-PI-004</p>	





ALWAYS THINK SAFETY	
UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS	
CASS SOFTWARE A/D AND D/A CONVERTER CALIBRATION	
DESIGNED: _____	TECHNICAL APPROVAL: _____
DRAWN: B.J. GARCIA	SUBMITTED: _____
CHECKED: T.V. _____	APPROVED: _____
DENVER, COLORADO	JAN. 1, 1991
CHIEF, ELECTRICAL BRANCH	
100-PI-006	

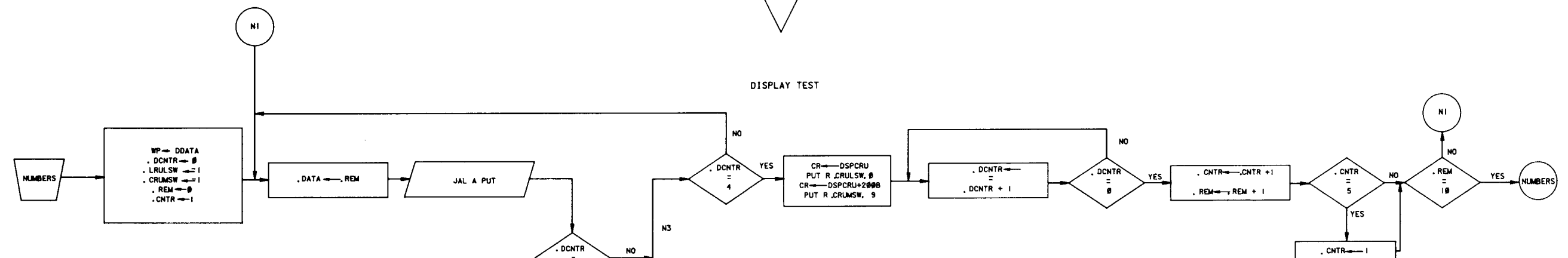
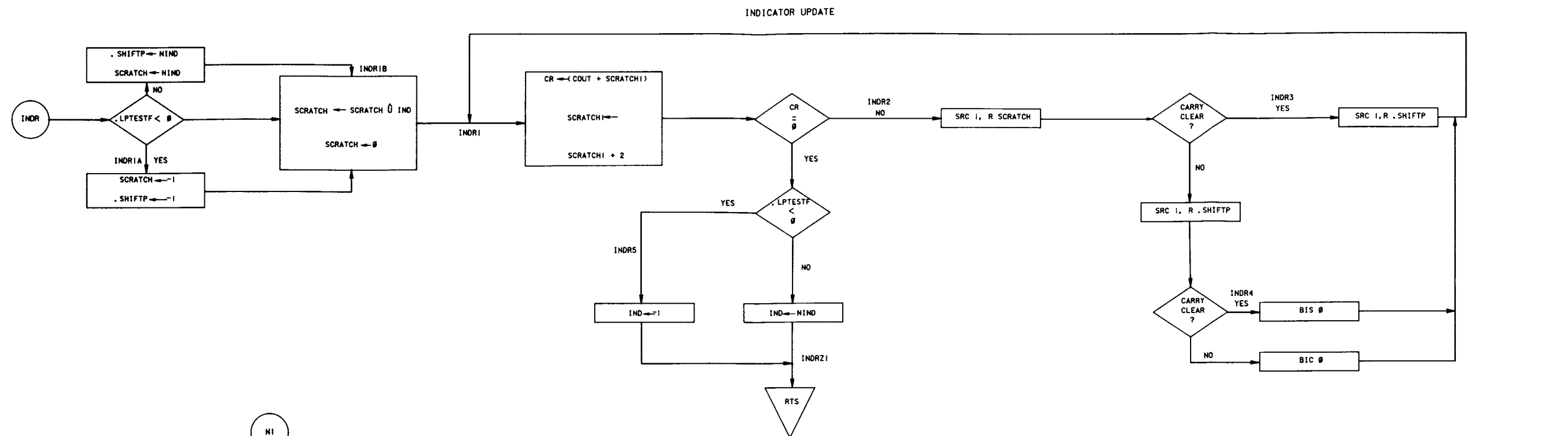


TABLE OF STATUS AND
LEDS-CRU LOCATIONS

COUT	OCT	1276	*SUBSTITUTE GENERATION*
	OCT	1240	*STATUS REQUEST*
	OCT	1242	*STATUS OF PMSC*
	OCT	1244	*BPA MW REQUEST*
	OCT	1246	*ANALOG NET GENERATION*
	OCT	1250	*PMSC NET GENERATION*
	OCT	1252	ALARM NO. 1
	OCT	1254	ALARM NO. 2
	OCT	1256	ALARM NO. 3
	OCT	1260	ALARM NO. 4
	OCT	1262	ALARM NO. 5
	OCT	1264	STATUS NO. 1
	OCT	1266	STATUS NO. 2
	OCT	1270	STATUS NO. 3
	OCT	1272	STATUS NO. 4
	OCT		

FRONT PANEL DRIVER WORKSPACE

PNLWP BSS 0
ALFLSH BSS 0
.SHIFTP EQU 0
.INDEX EQU 1
.LPTESTF EQU 2
.MFLG EQU 3
.INDDSP EQU 4
SCRATCH EQU 5
SCRATCH1 EQU 6
.ALIND EQU 7
.ALFLSH EQU 8
.NOUPD EQU 9
.FCNTR EQU 10
DISPDAT EQU 11

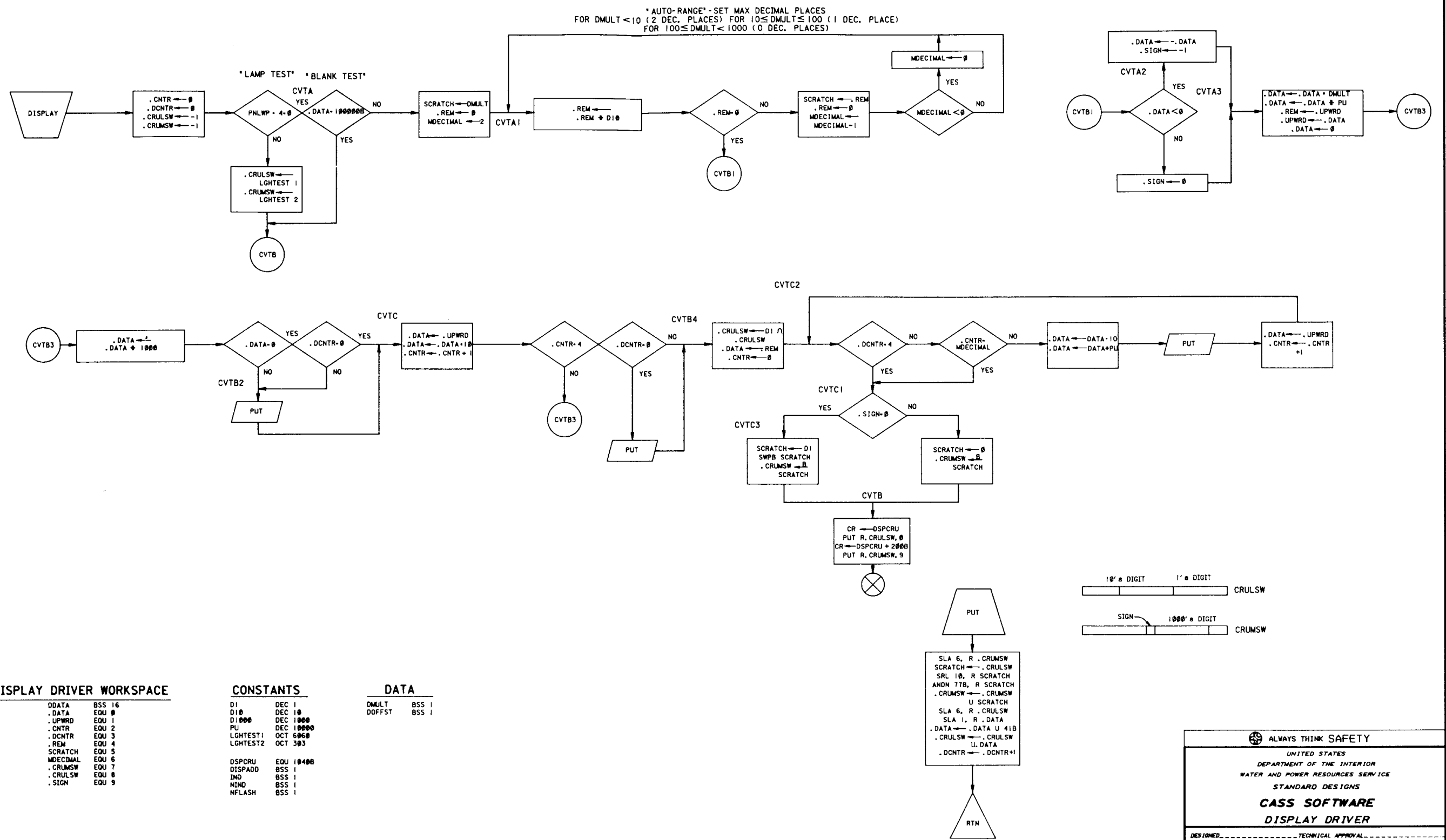
DISPLAY SUBROUTINE WORKSPACE

DDATA BSS 16
.DATA EQU 0
.UPWRD EQU 1
.CNTR EQU 2
.DCNTR EQU 3
.REM EQU 4
SCRATCH EQU 5
MDECIMAL EQU 6
.CRULSW EQU 8
.SIGN EQU 9

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UNITED STATES
DEPARTMENT OF THE INTERIOR
WATER AND POWER RESOURCES SERVICE
STANDARD DESIGNS
CASS SOFTWARE
FRONT PANEL DRIVER
SHEET 2

DESIGNED: _____ TECHNICAL APPROVAL: _____
DRAWN: T.V. C.W. 0010 SUBMITTED: _____
CHECKED: T.V. APPROVED: _____
DENVER, COLORADO JAN. 1, 1981 100-PI-008



DISPLAY DRIVER WORKSPACE

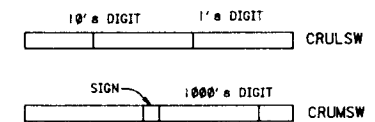
.DATA BSS 16
 .DCNTR EQU 0
 .UPWRD EQU 1
 .CNTR EQU 2
 .DCNTR EQU 3
 .REM EQU 4
 .SCRATCH EQU 5
 .MDECDMAL EQU 6
 .CRULSW EQU 7
 .CRULSW EQU 8
 .SIGN EQU 9

CONSTANTS

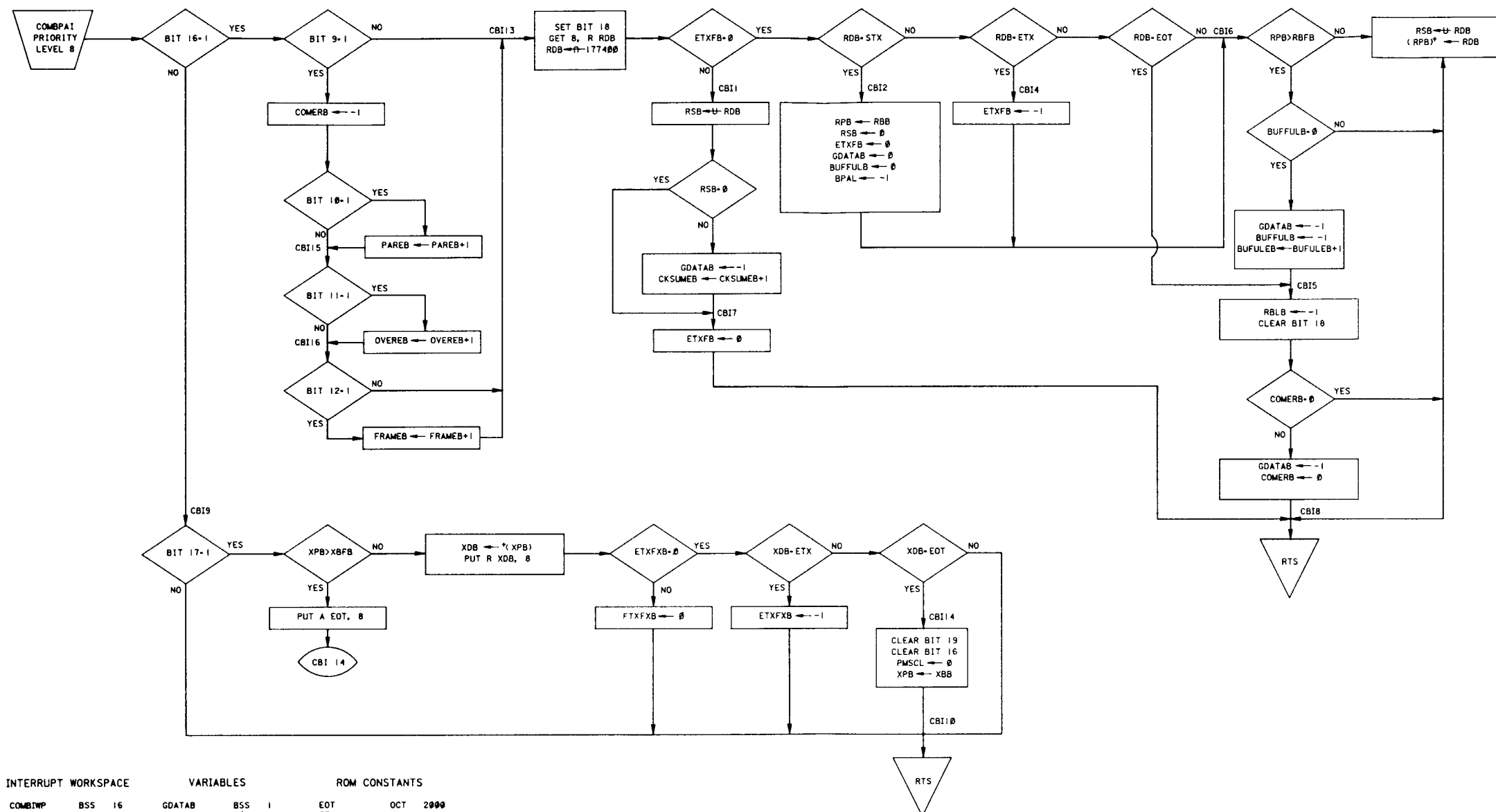
D1 DEC 1
 D10 DEC 10
 D1000 DEC 1000
 PU DEC 10000
 LGHTEST1 OCT 6060
 LGHTEST2 OCT 303
 DSPCRU EQU 10400
 DISPAD BSS 1
 INO BSS 1
 NIND BSS 1
 NFLASH BSS 1

DATA

DMULT BSS 1
 DOFFST BSS 1



ALWAYS THINK SAFETY UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS CASS SOFTWARE DISPLAY DRIVER	
DESIGNED DRAWN CHECKED DENVER, COLORADO	TECHNICAL APPROVAL SUBMITTED APPROVED JAN. 1, 1981
100-PI-009	



INTERRUPT WORKSPACE

COMBTP
RDB
RPB
RSB
ETXFB
COMERB
BUFFULB
XPB
XDB
ETXFXB

VARIABLES

BSS 16
GDATEB
RBLB
BPAL
CKSUMEB
PAREB
FRAMEB
OVEREB
BUFFULEB
RDB
XBB

ROM CONSTANTS

EOT OCT 2000
ETX OCT 1400
STX OCT 1000

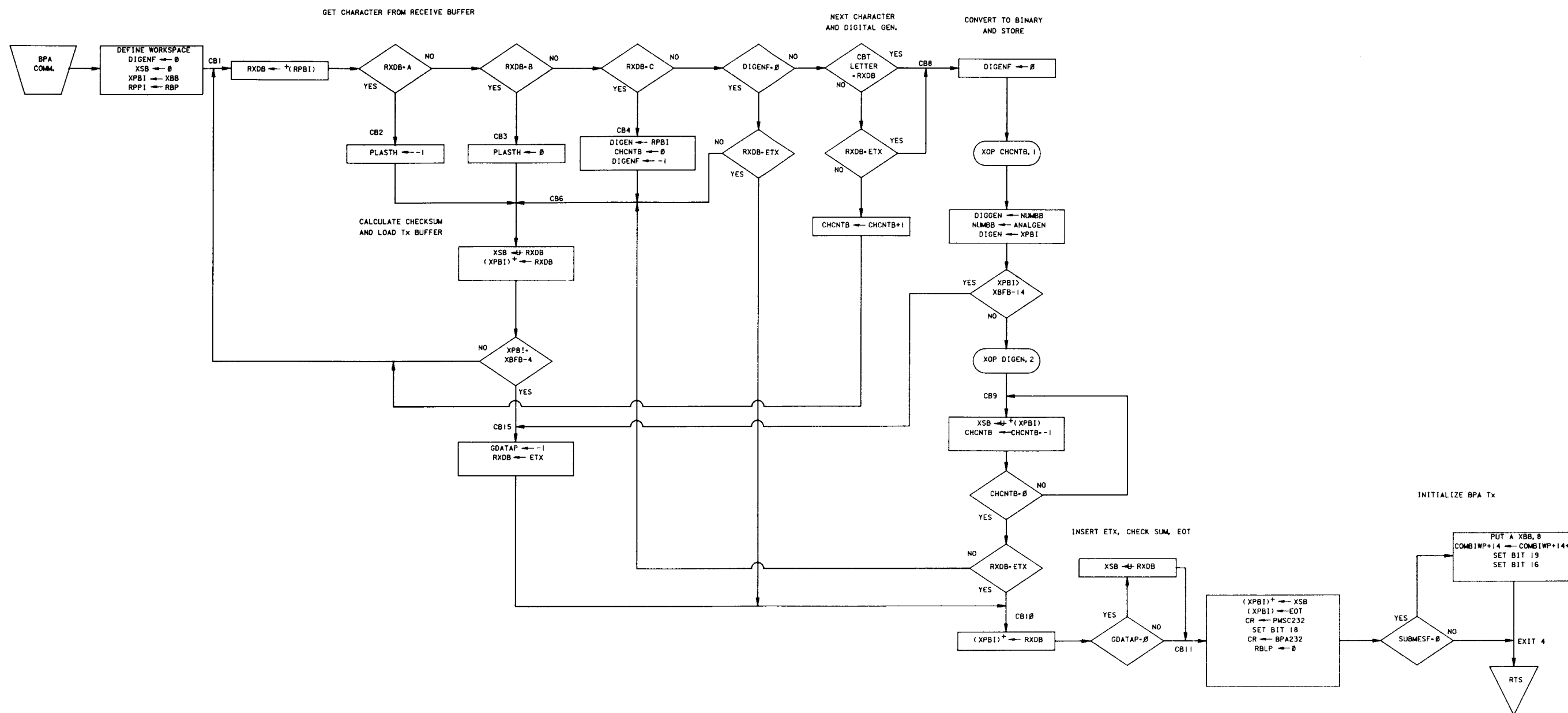
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UNITED STATES
DEPARTMENT OF THE INTERIOR
WATER AND POWER RESOURCES SERVICE
STANDARD DESIGNS

CASS SOFTWARE
BPA COMMUNICATIONS INTERRUPT
PRIORITY LEVEL 8

DESIGNED... TECHNICAL APPROVAL...
DRAWN... M.D. BUSTILLOS... SUBMITTED...
CHECKED... T.V... APPROVED...
DENVER, COLORADO JAN. 1, 1981

100-PI-010



ROM CONSTANTS

A	OCT	40400
B		41000
C		41400
BPA232		2000
PMS232		2200
EOT		2000
ETX		1400
LETTER		40000

WORKSPACE AND VARIABLES

COMBWP	BSS	16
RXDB	EQU	0
RPP1		2
XSB		3
XPB1		4
DIGENF		5
		6
		7
CHCNTB		8
DIGEN		9
NUMBB		10
PLASTH	BSS	1
DIGEN	BSS	1

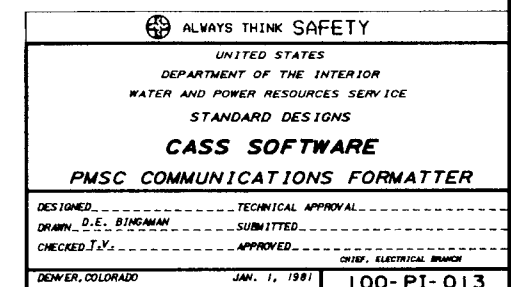
ALWAYS THINK SAFETY

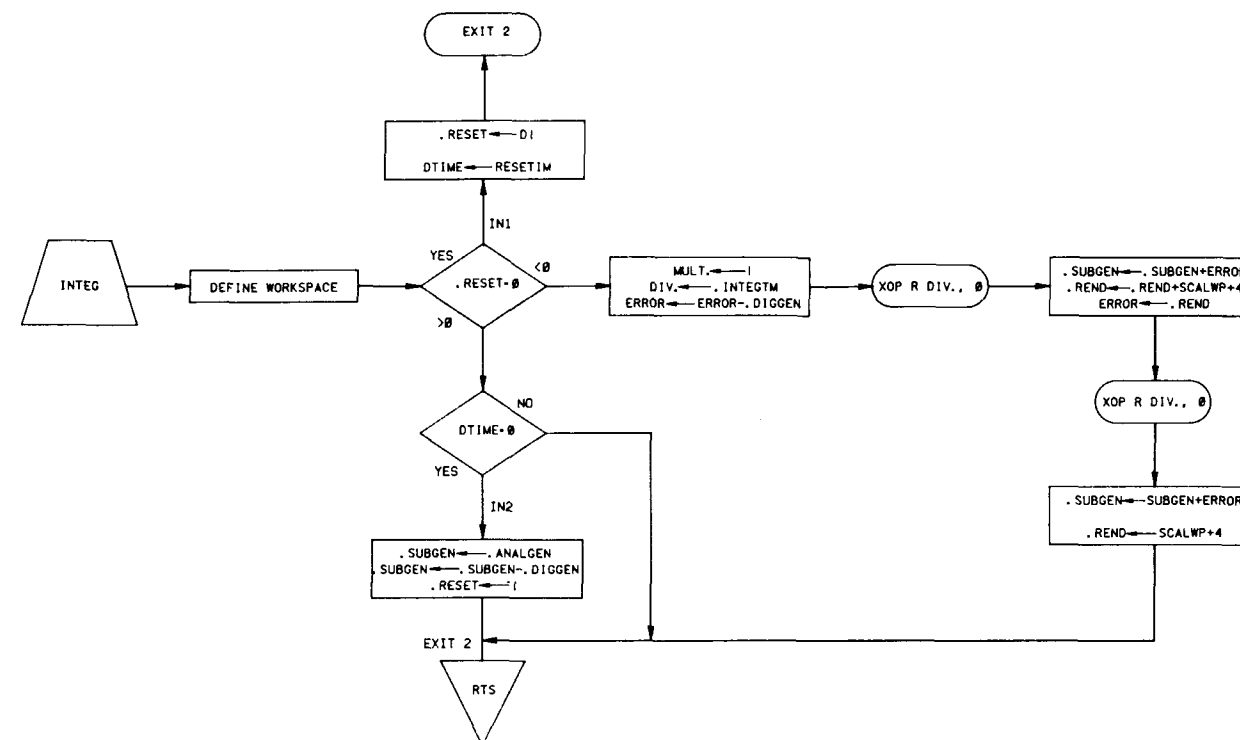
UNITED STATES
DEPARTMENT OF THE INTERIOR
WATER AND POWER RESOURCES SERVICE
STANDARD DESIGNS

CASS SOFTWARE
BPA COMMUNICATIONS FORMATTER

DESIGNED _____ TECHNICAL APPROVAL _____
DRAWN _____ SUBMITTED _____
CHECKED _____ APPROVED _____
CHIEF, ELECTRICAL BRANCH

DENVER, COLORADO JAN. 1, 1981 100-PI-011

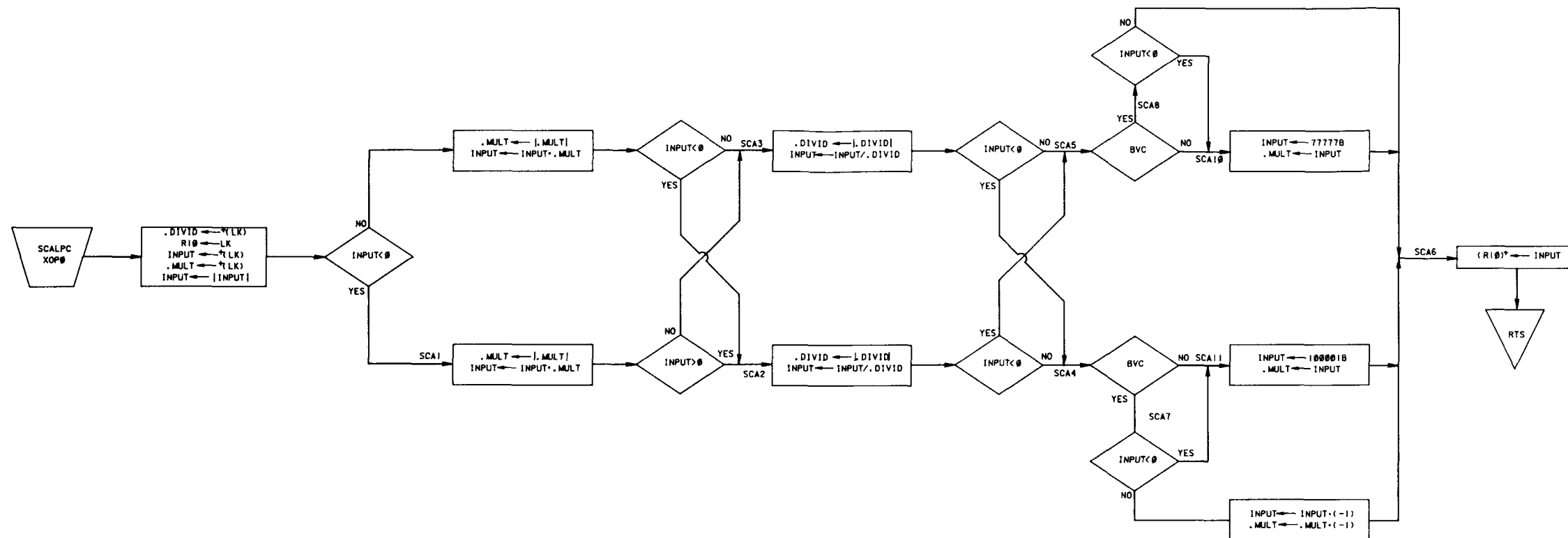




INTEGRATE WORKSPACE			EQUIVLENTS		
INTEGWP	EQU	#	.RESET	EQU	0
RESET	BSS	1	.INTEGTM		1
INTEGTM		1	.ANALGEN		2
ANALGEN		1	.DIGGEN		3
DIGGEN		1	.SUBGEN		4
SUBGEN		1	.REND		5
REND		1	.ANALCAL		6
ANALCAL		1	.RESETIM		7
RESETIM		9	DIV.		8
SCALWP		16	ERROR		9
			MULT.		10

ALWAYS THINK SAFETY UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS CASS INTEGRATOR DERIVES SUBSTITUTE GENERATION CASS SOFTWARE	
DESIGNED	TECHNICAL APPROVAL
DRAWN T.V.	C.W. Dp10 SUBMITTED
CHECKED T.V.	APPROVED
DENVER, COLORADO	JAN. 1, 1981

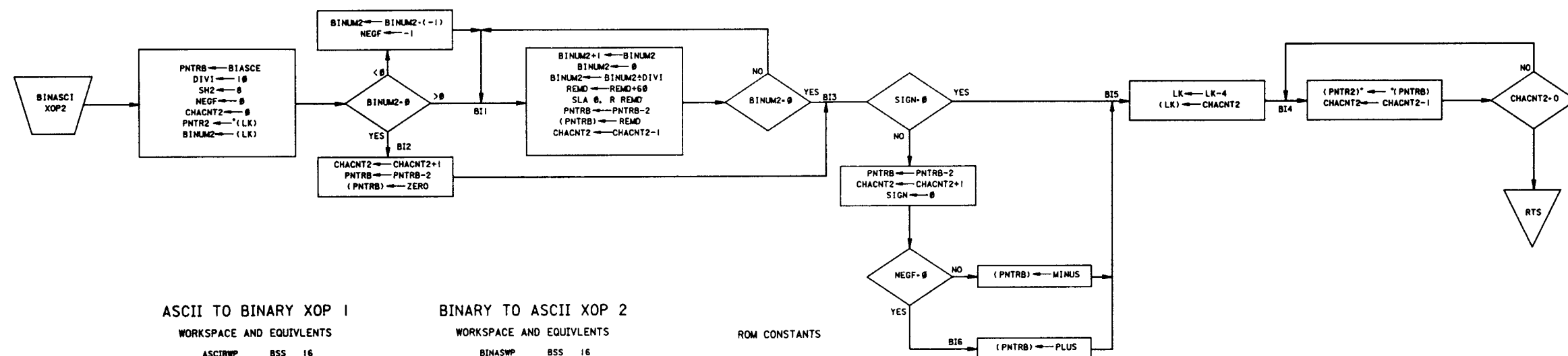
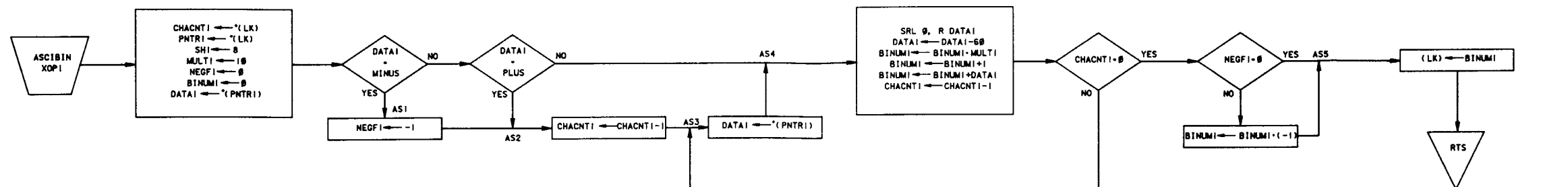
100-PI-014



SCALE XOP 0
WORKSPACE AND EQUIVALENTS

SCALWP	BSS	16
.DIVID	EQU	0
INPUT	EQU	1
.MULT	EQU	2
LK	EQU	11

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UNITED STATES	
DEPARTMENT OF THE INTERIOR	
WATER AND POWER RESOURCES SERVICE	
STANDARD DESIGNS	
CASS SOFTWARE	
SCALE XOP 0	
(R9+R10) / R8	
DESIGNED	TECHNICAL APPROVAL
DRAWN: M.D. JUSTILLOS	SUBMITTED
CHECKED: T.Y.	APPROVED
DENVER, COLORADO	CHIEF, ELECTRICAL BRANCH
JAN. 1, 1981	100-PI-016



ASCII TO BINARY XOP 1

WORKSPACE AND EQUIVLENTS

ASCIIWP	BSS	16
SH1	EQU	8
CHACNT1		1
PNTR1		2
DATA		3
MULT1		4
BINUM1		5
NEGF1		7
LK	EQU	11

BINARY TO ASCII XOP 2

WORKSPACE AND EQUIVLENTS

BINASWP	BSS	16
SH2	EQU	8
CHACNT2		1
PNTR2		2
PNTRB		3
BINUM2		4
REMO		5
DIV1		6
NEGF	EQU	7
SIGN	BSS	1
BIASC	BSS	6
BIASCE	EQU	11

ROM CONSTANTS

D10	DEC	10
MINUS	OCT	26400
PLUS	OCT	25400
ZERO	OCT	30000

ALWAYS THINK SAFETY UNITED STATES DEPARTMENT OF THE INTERIOR WATER AND POWER RESOURCES SERVICE STANDARD DESIGNS CASS SOFTWARE ASCII TO BINARY XOP1 BINARY TO ASCII XOP2	
DESIGNED	TECHNICAL APPROVAL
DRAWN	SUBMITTED
CHECKED	APPROVED
DENVER, COLORADO JAN. 1, 1981 100-PI-017	

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