A SIMPLIFIED FREQUENCY DEVIATION TRANSDUCER

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A Simplified Frequency Deviation Transducer

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A frequency deviation transducer with fast response has been developed using period comparison in CMOS and analog logic. The transducer is useful in monitoring frequency where frequency deviation is important and long-term accuracy is not required.

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by

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INTRODUCTION

In the early 1970's, a frequency-deviation transducer that was fast and ripple free was developed for use in control applications to improve power system dynamics. In succeeding years, several frequency-deviation transducers with different theories of operation and circuit techniques were built and tested. This report describes the latest model.

CONCLUSIONS

1. A simplified fast response frequency-deviation transducer has been developed for relaying and continuous control applications in power systems.

2. Improved reliability resulted from reducing the parts count by half, allowing a single-card unit.

3. A simplified alignment procedure resulted from reducing the number of trimming potentiometers from six to three.

4. CMOS technology reduces the power requirement from 2 watts to less than 0.5 watt.

5. Output ripple is reduced to 5 millivolts peak to peak for any constant frequency within the operating range.

GENERAL PRINCIPLE

This transducer measures frequency deviation by comparing the period of the measured waveform to a constant reference period generated within the transducer. The period of the applied waveform is determined by a zero crossing detector, and the reference period is generated by two precision monostable multivibrators (one shots). The waveform \( Q_g \) (fig. 1) is the zero crossing detector output. The rising edge of \( Q_g \) triggers the first one shot (OS1, fig. 2) via ENs, generating a constant width pulse \( Q_1 \). The rising edge of \( Q_1 \) in turn initiates a similar constant width pulse \( Q_2 \). The time between the rising edge of \( Q_1 \) and the following negative going edge of \( Q_2 \) is the constant reference period mentioned previously. Any positive frequency deviation of the unknown signal \( Q_s \) is detected by applying \( Q_1 \) and \( Q_2 \) to the NAND gate \( N_1 \) (fig. 2). Positive frequency deviation results in a period reduction of \( Q_s \). Positive frequency deviation (high frequency) produces the output

\[
Q_{dh} = Q_1Q_2
\]

from the associated enable gate \( EN_1 \). When positive deviation exists as illustrated in the high-frequency portions of \( Q_s \), \( Q_1 \) and \( Q_2 \) are both positive for a time proportional to the magnitude of the period deviation. For the condition of no deviation or negative deviation, an inspection shows that \( Q_1 \) and \( Q_2 \) are never positive at the same time; therefore, gate \( N_1 \) will not respond to negative frequency swings.

Negative deviation is detected similarly by applying \( Q_1 \) and \( Q_2 \) to NAND gate \( N_2 \). Inspection of \( Q_1 \) and \( Q_2 \) reveals that a signal proportional to negative period deviation results from this process and conversely gate \( N_2 \) and \( EN_2 \) will not respond to positive deviation. This signal is:

\[
Q_{dl} = \overline{Q_1Q_2}
\]

It now remains to convert the variable pulse width of \( Q_{dh} \) or \( Q_{dl} \) to an appropriate d-c level. The pulse width d-c conversion is accomplished by using the pulses \( Q_{dl} \) or \( Q_{dh} \) to gate on a constant rate integrator \( I \), via enabling NAND gates \( EN_1 \) and \( EN_2 \) (fig. 2). The integrator responds in a positive direction for positive deviation and conversely for negative swings. The final value of the linear ramp thus generated is proportional to period deviation and is converted to d-c by a sample hold circuit. This process results in a fast response (18 ms) and low-ripple (5-mV) d-c output. The integrator is reset after each sample is taken. Because the d-c output is proportional to period deviation, which is the reciprocal of frequency deviation, there is an inherent nonlinearity; however, the error is insignificant over the frequency range of interest (55-65 Hz). The enabling NAND gates \( EN_1 \), through \( EN_2 \) together with \( ST_1 \) and \( ST_2 \), form a fail-safe system which causes the frequency transducer to fail to a 0 volt output with loss of signal.

CIRCUIT DESCRIPTIONS

Input Filter and Zero Crossing Detector

The input filter (R7, Rs, and C5) protects the comparator (A3) from transients and has a time constant of approximately 1.7 milliseconds. The comparator acts as a zero crossing detector and also prevents application of the input signal to the CMOS circuits when the CMOS d-c power source is off.

One section of a 4093 CMOS Schmitt trigger (EN4) is used as an enabling gate generating a proper fast rise time signal for triggering the following CMOS monostable multivibrator. The period of the Schmitt trigger output (waveform Qs of fig. 1) equals the period of the applied 60-Hz sine wave.

Period Sensing Multivibrators (One Shots)

The first one shot (OS1) is triggered by the positive transitions of the waveform Qs (fig. 1) resulting in a constant width pulse Q1 (fig. 1). The width of Q1 is determined primarily by capacitor C1 together with resistor R1 and trimmer R2 (fig. 3).

The second one shot (OS2) is identical but is triggered by the positive transition of Q1 generating a constant width pulse Q2. The timing of Q2 is determined by C2 in conjunction with R3 and Rs. The fixed timing of OS2 is selected for a nearly symmetrical square wave at the calibrated frequency (60 Hz) by selecting Rs. Trimmer R2 for OS1 allows matching of the constant width portion of Q1 to the variable portion of Q2 at 60 Hz and is thus a frequency calibration adjustment.

The error or deviation waveform Qdh or Qdl is present only when the frequency deviates from 60 Hz. Signals Qdl or Qdh are generated by applying the appropriate one-shot outputs to AND gates. The AND function is implemented using two NAND gates (N1 together with EN1 and N2 with EN2).

Period Deviation Detection NAND Gates

Gates N1 and N2 are CMOS two-input NAND Schmitt triggers. Their function is to generate a precise pulse in response to any deviation in the period (frequency) of the applied waveform. They operate as conventional NAND gates; therefore, their operation is not described here. It is only necessary to be aware of the source of their inputs and to understand how the gates detect period deviation. This detection method is readily understood by inspection of the input waveforms. Signals Q1 and Q2 go to gate N1 for detection of positive deviation (high frequency) and Q1 and Q2 go to gate N2 for negative deviation. Gates N1 and N2 respond only when the inputs are simultaneously high. The timing diagram shows the response of each gate to these conditions and illustrates that gates N1 and N2 only respond to the corresponding positive or negative deviation, respectively. The resulting NAND gate outputs operate analog switches SW1 and SW2 via enabling NAND gates EN1 and EN2. The enabling gates ensure a 0 volt output of the frequency transducer for loss of the 60-Hz input signal.

D-C Reference Source

The stable positive d-c reference voltage is derived by an Analog Devices AD 584 reference regulator. It is an integrated circuit and is described in technical specification manuals published by the manufacturer. The negative reference voltage is generated by inverting the positive reference via a unity gain inverting amplifier A2, resulting in a “tracking” positive and negative reference. The reference voltages are applied to the integrator via analog switches SW1 and SW2.

Analog Switch and Integrator

The quad analog switch is an integrated circuit which serves three purposes: SW1 and SW2 apply the d-c reference voltage to the integrator I1. SW3 resets the integrator after each integration cycle, and SW4 samples the integrator output at the appropriate time. The salient feature in the operation of this switch is the relative timing of the integration period, the sample timing, and the reset. The integrator responds with either a positive or negative constant integration rate determined by applying the stable positive or negative reference voltage to its input. When there is no deviation, both Qdh and Qdl are low, therefore both SW1 and SW2 are open. This results in a 0-volt input to the integrator. Trimming potentiometer Rs nullifies any tendency of the integrator to drift with a 0-volt input.
If a frequency deviation occurs, the appropriate NAND gate (Ni or N2) output goes low (ENi or EN2 goes high), thus connecting the negative or positive reference voltage to the integrator I1 causing the integrator output to slew in the appropriate direction.

The integrator responds for a time determined by the width of the Qn or Qp pulse. The width of Qn or Qp is proportional to the deviation of the period of the signal Qt applied to the transducer. Therefore, the final value of the integrator ramp is proportional to the period deviation in question. The integrator holds the final value while the sample is immediately taken by the sample hold circuit.

**Fail-safe Circuits**

The effect on the output voltage of this transducer with loss of the 60-Hz input signal is not predictable. Therefore, a number of enabling gates in the form of two input NAND Schmitt triggers are used which cause the sample hold output to always fall to 0 volt when the 60-Hz input falls below a predetermined level. The enabling gates are EN1 through EN4. One input of all the gates is hooked to a common enable bus. When this bus voltage is high, each gate will pass its corresponding signal. When the bus goes low, all gate outputs remain high, causing SW1 through SW4 to close simultaneously, and the one shots are no longer triggered. Inspection of figure 3 reveals that, under this condition, the integrator (I1) and sample hold (A1) become a low gain (less than 0.17) system with 0 net input and therefore 0 output. The bus voltage is developed by transistor TR1, driving two cascaded Schmitt triggers ST1 and ST2. If the 60-Hz input signal is sufficiently large to trigger ST1, and thus ST2, either the ST1 or ST2 output will be high at any given time. The two outputs feed the enable bus through a two-input diode OR gate keeping the bus high. If the 60-Hz signal falls below about 6 volts peak, ST1 will no longer trigger and its output will go low. Likewise, the output of ST2 goes low because of the capacitive coupling of ST1 to ST2. This allows the enable bus to stay low, causing the transducer to reliably fail to a 0 volt output.

**Sample Hold Circuit**

The sample hold circuit is made up of SW4, R20, R21, C8, and A1. The timing of the sample is critical and is controlled by one shot OS1 triggered by the output of NAND gate N2. Inspection of the timing diagram reveals how Q1 and Q2 are used via N3 to generate a sample trigger. Amplifier A1 (fig. 3) is an FET input noninverting amplifier used to isolate the transducer load from the hold capacitor C8. Trimming resistor R23 adjusts the gain of A1 and is used to adjust the transducer output resolution to 2 V/Hz. After the sample is taken, the integrator is reset by the reset one shot OS4 via EN4 and SW3.

**Sample and Reset One Shots**

The reset one shot OS4 is half of a dual 4538 CMOS unit as is the sample one shot OS3 described previously. The timing for OS3 is R6 and C8, while R6 and C8 control OS4.

**Alignment and Calibration**

Alignment and calibration of this single-card version are greatly simplified as compared to the three-card system. Initially, the integrator drift trimmer R28 is set to 0 volt on the wiper and 60 Hz is applied to the transducer. If available, the 60-Hz source should be derived by dividing down a crystal oscillator, although for frequency deviation use such as in power system stabilizers, the line frequency under normal operating conditions is adequate.

With 60 Hz applied, R3 is adjusted for 0 volt out of the transducer. Next, observe the output of the integrator with an oscilloscope and adjust R23 to remove any apparent sawtooth waveform. (Use maximum scope sensitivity for this adjustment.) The final adjustment is R23 which calibrates the output to -1.96 volts at 59 Hz and +2.03 volts at 61 Hz. The accuracy realized in this calibration procedure is, of course, limited by the accuracy of the variable frequency source used; however, the requirements are identical to those for the three-card system.

**SPECIFICATIONS**

**Input**

The input transformer may be selected to meet particular situations providing the secondary produces 12 volts rms at 10 milliamperes. Standard ranges of 67, 115, or 230 volts input.
are usually used. The frequency may range from 55 to 65 Hz.

**Output**

Normally the output is 2.0 V/Hz deviation from 60 Hz bipolar with positive polarity for frequencies above 60 Hz and negative below 60 Hz with one terminal grounded. The calibration range is ±10 percent.

**Ripple**

Less than 5 millivolts peak to peak with constant frequency input.

**Response Time**

The response time equals the reference period +0.5 millisecond for frequencies equal to or greater than 60 Hz and is equal to the applied period +0.5 millisecond for frequencies below 60 Hz.

**Sensitivity to Input Signal Level**

Indistinguishable from noise down to 0.3 PU. Below 0.3 PU input the transducer fails to a 0 volt output.

**Temperature Range**

0 to 50 °C.

**Burden**

Less than 0.1 volt ampere at the PT input maximum.

**Power Requirements**

Plus and minus 15 volts d.c. at less than 15 milliamperes.
Figure 1.—Transducer waveforms and relationships.
Figure 2.—Block diagram of frequency transducer.
Figure 3.—Schematic diagram.
Figure 4.—Power distribution.
Figure 5—Gain and phase response.
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