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A SIMPLIFIED FREQUENCY DEVIATION TRANSDUCER

November 1981

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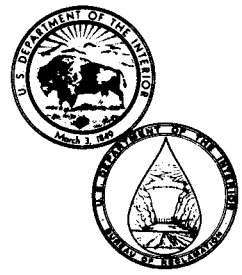

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16. ABSTRACT

A frequency deviation transducer with fast response has been developed using period comparison in CMOS and analog logic. The transducer is useful in monitoring frequency where frequency deviation is important and long-term accuracy is not required.

17. KEY WORDS AND DOCUMENT ANALYSIS

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b. IDENTIFIERS-- frequency deviation transducer/ electronic circuit

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by

Eugene Campbell and James R. Schurz

November 1981

Power and Instrumentation Branch
Division of Research
Engineering and Research Center
Denver, Colorado

SI METRIC

UNITED STATES DEPARTMENT OF THE INTERIOR • BUREAU OF RECLAMATION

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CONTENTS

FIGURES

INTRODUCTION

In the early 1970's, a frequency-deviation transducer that was fast and ripple free was developed for use in control applications to improve power system dynamics. [1] In succeeding years, several frequency-deviation transducers with different theories of operation and circuit techniques were built and tested. This report describes the latest model.

CONCLUSIONS

1. A simplified fast response frequency-deviation transducer has been developed for relaying and continuous control applications in power systems.

2. Improved reliability resulted from reducing the parts count by half, allowing a single-card unit.

3. A simplified alinement procedure resulted from reducing the number of trimming potentiometers from six to three.

4. CMOS technology reduces the power requirement from 2 watts to less than 0.5 watt.

5. Output ripple is reduced to 5 millivolts peak to peak for any constant frequency within the operating range.

GENERAL PRINCIPLE

This transducer measures frequency deviation by comparing the period of the measured waveform to a constant reference period generated within the transducer. The period of the applied waveform is determined by a zero crossing detector, and the reference period is generated by two precision monostable multivibrators (one shots). The waveform Q_s (fig. 1) is the zero crossing detector output. The rising edge of Q_s triggers the first one shot (OS_1, fig. 2) via EN_5, generating a constant width pulse Q_1. The rising edge of Q_1 in turn initiates a similar constant width pulse Q_2. The time between the rising edge of Q_1 and the following negative going edge of Q_2 is the constant reference period mentioned previously. Any positive frequency deviation of the unknown signal Q_s is detected by applying Q_1 and Q_2 to the NAND gate N_1 (fig. 2). Positive frequency deviation results in a period reduction of Q_s. Positive frequency deviation (high frequency) produces the output

$$Q_{dh} = Q_1 Q_2$$

from the associated enable gate EN_1. When positive deviation exists as illustrated in the high-frequency portions of Q_s, Q_1 and Q_2 are both positive for a time proportional to the magnitude of the period deviation. For the condition of no deviation or negative deviation, an inspection shows that Q_1 and Q_2 are never positive at the same time; therefore, gate N_1 will not respond to negative frequency swings.

Negative deviation is detected similarly by applying Q_1 and Q_2 to NAND gate N_2. Inspection of Q_1 and Q_2 reveals that a signal proportional to negative period deviation results from this process and conversely gate N_2 and EN_2 will not respond to positive deviation. This signal is:

$$Q_{dL} = \overline{Q_1}\,\overline{Q_2}.$$

It now remains to convert the variable pulse width of Q_{dh} or Q_{dL} to an appropriate d-c level. The pulse width d-c conversion is accomplished by using the pulses Q_{dL} or Q_{dh} to gate on a constant rate integrator I_1 via enabling NAND gates EN_1 and EN_2 (fig. 2). The integrator responds in a positive direction for positive deviation and conversely for negative swings. The final value of the linear ramp thus generated is proportional to period deviation and is converted to d.c. by a sample hold circuit. This process results in a fast response (18 ms) and low-ripple (5-mV) d-c output. The integrator is reset after each sample is taken. Because the d-c output is proportional to period deviation, which is the reciprocal of frequency deviation, there is an inherent nonlinearity; however, the error is insignificant over the frequency range of interest (55-65 Hz). The enabling NAND gates (EN_1 through EN_6) together with ST_1 and ST_2, form a fail-safe system which causes the frequency transducer to fail to a 0 volt output with loss of signal.

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[1] Gish, W. B., C. L. Clemans, and F. R. Schleif, A Frequency Deviation Transducer with Fast Response, Research Report REC-ERC-71-24, Bureau of Reclamation, May 1971.

CIRCUIT DESCRIPTIONS

Input Filter and Zero Crossing Detector

The input filter (R_7, R_8, and C_5) protects the comparator (A_3) from transients and has a time constant of approximately 1.7 milliseconds. The comparator acts as a zero crossing detector and also prevents application of the input signal to the CMOS circuits when the CMOS d-c power source is off.

One section of a 4093 CMOS Schmitt trigger (EN_5) is used as an enabling gate generating a proper fast rise time signal for triggering the following CMOS monostable multivibrator. The period of the Schmitt trigger output (waveform Q_s of fig. 1) equals the period of the applied 60-Hz sine wave.

Period Sensing Multivibrators (One Shots)

The first one shot (OS_1) is triggered by the positive transitions of the waveform Q_s (fig. 1) resulting in a constant width pulse Q_1 (fig. 1). The width of Q_1 is determined primarily by capacitor C_1 together with resistor R_1 and trimmer R_2 (fig. 3).

The second one shot (OS_2) is identical but is triggered by the positive transition of Q_1 generating a constant width pulse Q_2. The timing of Q_2 is determined by C_2 in conjunction with R_3 and R_4. The fixed timing of OS_2 is selected for a nearly symmetrical square wave at the calibrated frequency (60 Hz) by selecting R_4. Trimmer R_2 for OS_1 allows matching of the constant width portion of Q_1 to the variable portion of Q_2 at 60 Hz and is thus a frequency calibration adjustment.

The error or deviation waveform Q_{dh} or Q_{dL} is present only when the frequency deviates from 60 Hz. Signals Q_{dL} or Q_{dh} are generated by applying the appropriate one-shot outputs to AND gates. The AND function is implemented using two NAND gates (N_1 together with EN_1 and N_2 with EN_2).

Period Deviation Detection NAND Gates

Gates N_1 and N_2 are CMOS two-input NAND Schmitt triggers. Their function is to generate a precise pulse in response to any deviation in the period (frequency) of the applied waveform. They operate as conventional NAND gates; therefore, their operation is not described here. It is only necessary to be aware of the source of their inputs and to understand how the gates detect period deviation. This detection method is readily understood by inspection of the input waveforms. Signals Q_1 and Q_2 go to gate N_1 for detection of positive deviation (high frequency) and Q_1 and Q_2 go to gate N_2 for negative deviation. Gates N_1 and N_2 respond only when the inputs are simulataneously high. The timing diagram shows the response of each gate to these conditions and illustrates that gates N_1 and N_2 only respond to the corresponding positive or negative deviation, respectively. The resulting NAND gate outputs operate analog switches SW_1 and SW_2 via enabling NAND gates EN_1 and EN_2. The enabling gates ensure a 0 volt output of the frequency transducer for loss of the 60-Hz input signal.

D-C Reference Source

The stable positive d-c reference voltage is derived by an Analog Devices AD 584 reference regulator. It is an integrated circuit and is described in technical specification manuals published by the manufacturer. The negative reference voltage is generated by inverting the positive reference via a unity gain inverting amplifier A_2, resulting in a "tracking" positive and negative reference. The reference voltages are applied to the integrator via analog switches SW_1 and SW_2.

Analog Switch and Integrator

The quad analog switch is an integrated circuit which serves three purposes: SW_1 and SW_2 apply the d-c reference voltage to the integrator I_1, SW_3 resets the integrator after each integration cycle, and SW_4 samples the integrator output at the appropriate time. The salient feature in the operation of this switch is the relative timing of the integration period, the sample timing, and the reset. The integrator responds with either a positive or negative constant integration rate determined by applying the stable positive or negative reference voltage to its input. When there is no deviation, both Q_{dh} and Q_{dL} are low, therefore both SW_1 and SW_2 are open. This results in a 0-volt input to the integrator. Trimming potentiometer R_{26} nullifies any tendency of the integrator to drift with a 0-volt input.

If a frequency deviation occurs, the appropriate NAND gate (N_1 or N_2) output goes low (EN_1 or EN_2 goes high), thus connecting the negative or positive reference voltage to the integrator I_1 causing the integrator output to slew in the appropriate direction.

The integrator responds for a time determined by the width of the Q_{dh} or Q_{dL} pulse. The width of Q_{dh} or Q_{dL} is proportional to the deviation of the period of the signal Q_s applied to the transducer. Therefore, the final value of the integrator ramp is proportional to the period deviation in question. The integrator holds the final value while the sample is immediately taken by the sample hold circuit.

Fail-safe Circuits

The effect on the output voltage of this transducer with loss of the 60-Hz input signal is not predictable. Therefore, a number of enabling gates in the form of two input NAND Schmitt triggers are used which cause the sample hold output to always fail to 0 volt when the 60-Hz input falls below a predetermined level. The enabling gates are EN_1 through EN_5. One input of all the gates is hooked to a common enable bus. When this bus voltage is high, each gate will pass its corresponding signal. When the bus goes low, all gate outputs remain high, causing SW_1 through SW_4 to close simultaneously, and the one shots are no longer triggered. Inspection of figure 3 reveals that, under this condition, the integrator (I_1) and sample hold (A_1) become a low gain (less than 0.17) system with 0 net input and therefore 0 output. The bus voltage is developed by transistor TR_1 driving two cascaded Schmitt triggers ST_1 and ST_2. If the 60-Hz input signal is sufficiently large to trigger ST_1 and thus ST_2, either the ST_1 or ST_2 output will be high at any given time. The two outputs feed the enable bus through a two-input diode OR gate keeping the bus high. If the 60-Hz signal falls below about 6 volts peak, ST_1 will no longer trigger and its output will go low. Likewise, the output of ST_2 goes low because of the capacitive coupling of ST_1 to ST_2. This allows the enable bus to stay low, causing the transducer to reliably fail to a 0 volt output.

Sample Hold Circuit

The sample hold circuit is made up of SW_4, R_{20}, R_{21}, C_8, and A_1. The timing of the sample is critical and is controlled by one shot OS_3 triggered by the output of NAND gate N_3. Inspection of the timing diagram reveals how Q_1 and Q_2 are used via N_3 to generate a sample trigger. Amplifier A_1 (fig. 3) is an FET input noninverting amplifier used to isolate the transducer load from the hold capacitor C_8. Trimming resistor R_{23} adjusts the gain of A_1 and is used to adjust the transducer output resolution to 2 V/Hz. After the sample is taken, the integrator is reset by the reset one shot OS_4 via EN_3 and SW_3.

Sample and Reset One Shots

The reset one shot OS_4 is half of a dual 4538 CMOS unit as is the sample one shot OS_3 described previously. The timing for OS_3 is R_5 and C_3, while R_6 and C_4 control OS_4.

Alinement and Calibration

Alinement and calibration of this single-card version are greatly simplified as compared to the three-card system. Initially, the integrator drift trimmer R_{26} is set to 0 volt on the wiper and 60 Hz is applied to the transducer. If available, the 60-Hz source should be derived by dividing down a crystal oscillator, although for frequency deviation use such as in power system stabilizers, the line frequency under normal operating conditions is adequate.

With 60 Hz applied, R_2 is adjusted for 0 volt out of the transducer. Next, observe the output of the integrator with an oscilloscope and adjust R_{26} to remove any apparent sawtooth waveform. (Use maximum scope sensitivity for this adjustment.) The final adjustment is R_{23} which calibrates the output to −1.96 volts at 59 Hz and +2.03 volts at 61 Hz. The accuracy realized in this calibration procedure is, of course, limited by the accuracy of the variable frequency source used; however, the requirements are identical to those for the three-card system.

SPECIFICATIONS

Input

The input transformer may be selected to meet particular situations providing the secondary produces 12 volts rms at 10 milliamperes. Standard ranges of 67, 115, or 230 volts input

are usually used. The frequency may range from 55 to 65 Hz.

Output

Normally the outout is 2.0 V/Hz deviation from 60 Hz bipolar with positive polarity for frequencies above 60 Hz and negative below 60 Hz with one terminal grounded. The calibration range is $\pm$10 percent.

Ripple

Less than 5 millivolts peak to peak with constant frequency input.

Response Time

The response time equals the reference period +0.5 millisecond for frequencies equal to or greater than 60 Hz and is equal to the applied period +0.5 millisecond for frequencies below 60 Hz.

Sensitivity to Input Signal Level

Indistinguishable from noise down to 0.3 PU. Below 0.3 PU input the transducer fails to a 0 volt output.

Temperature Range

0 to 50 °C.

Burden

Less than 0.1 volt ampere at the PT input maximum.

Power Requirements

Plus and minus 15 volts d.c. at less than 15 milliamperes.

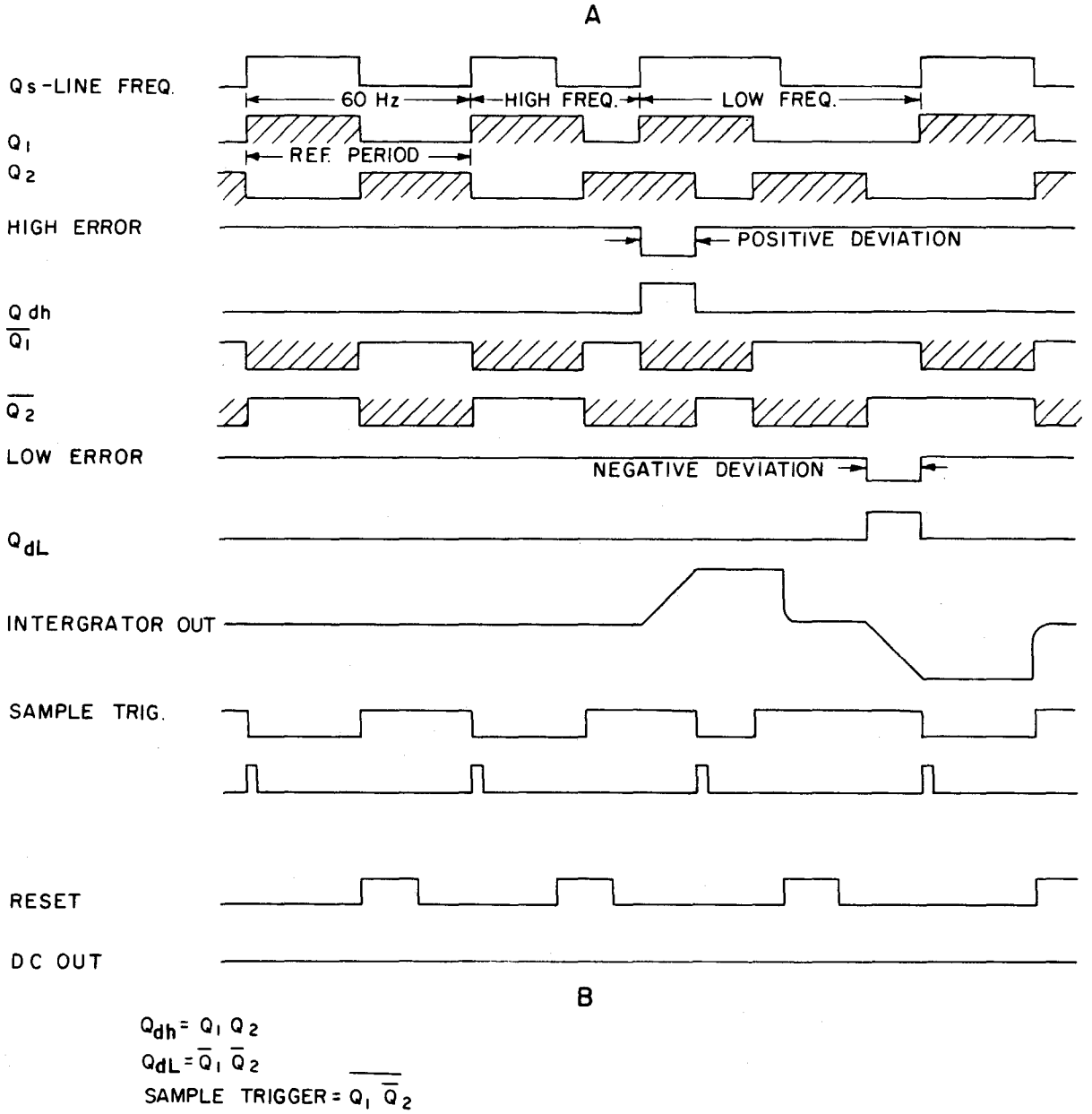

Figure 1.–Transducer waveforms and relationships.

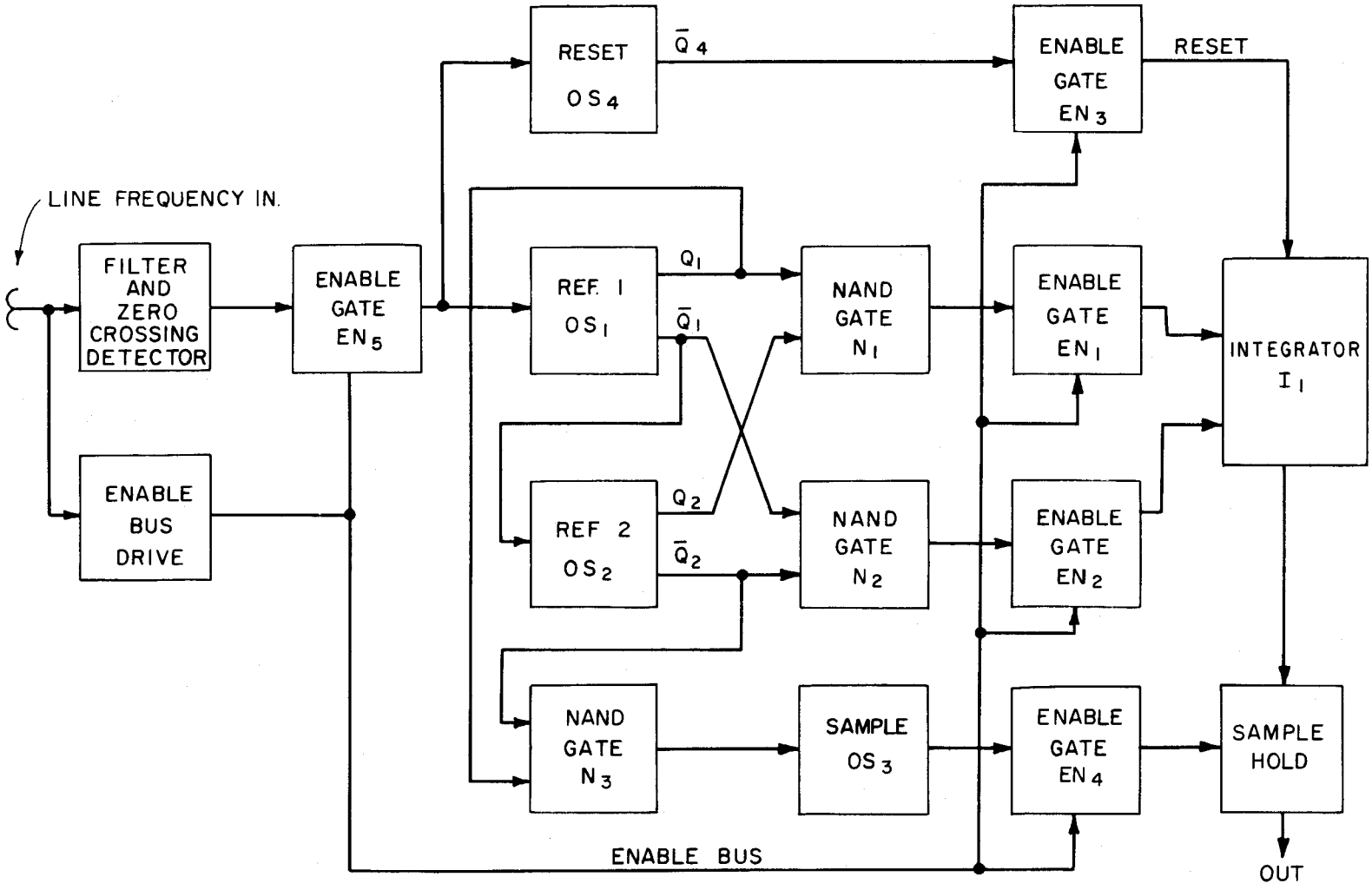

Figure 2.–Block diagram of frequency transducer.

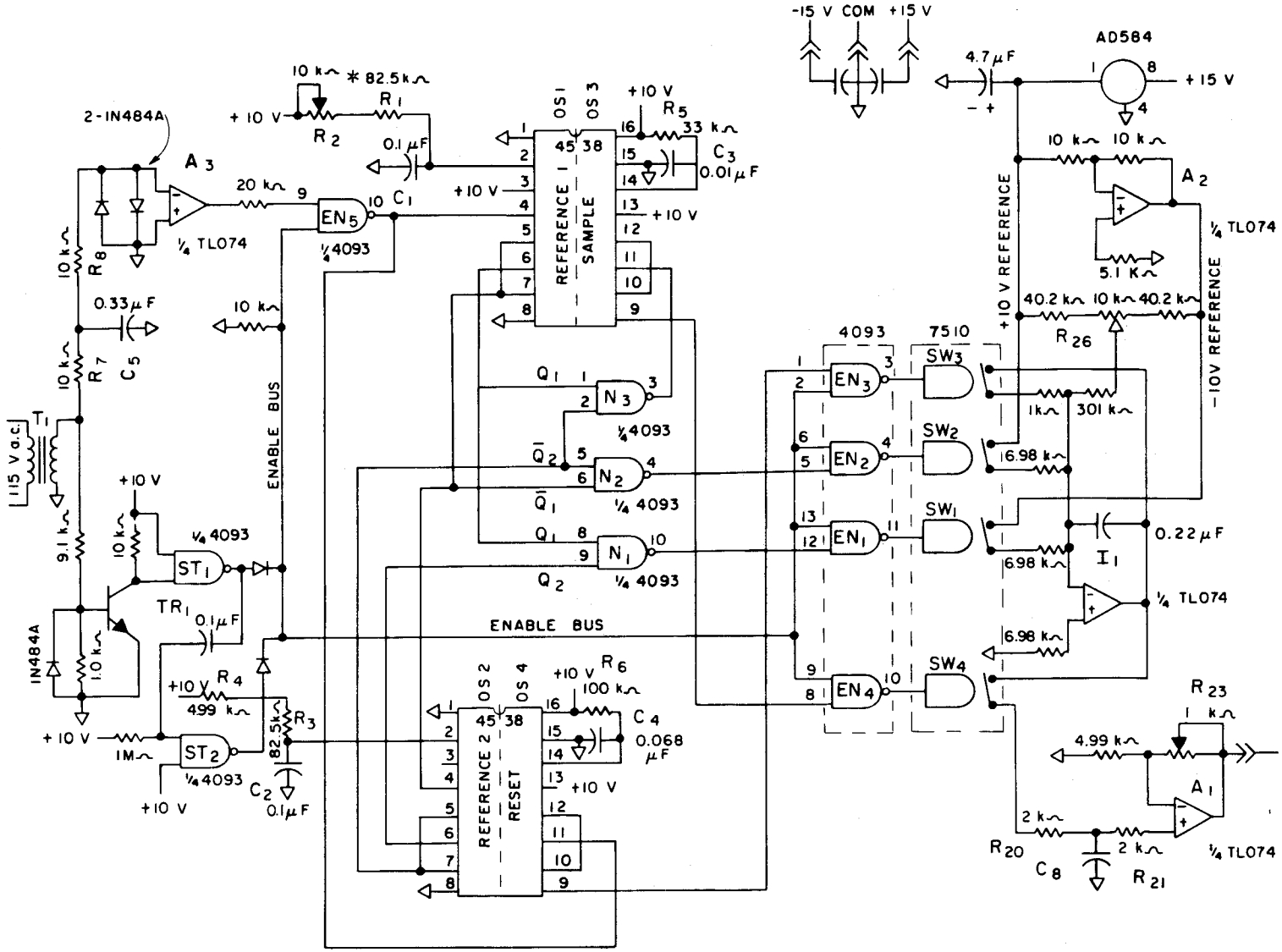

Figure 3.–Schematic diagram.

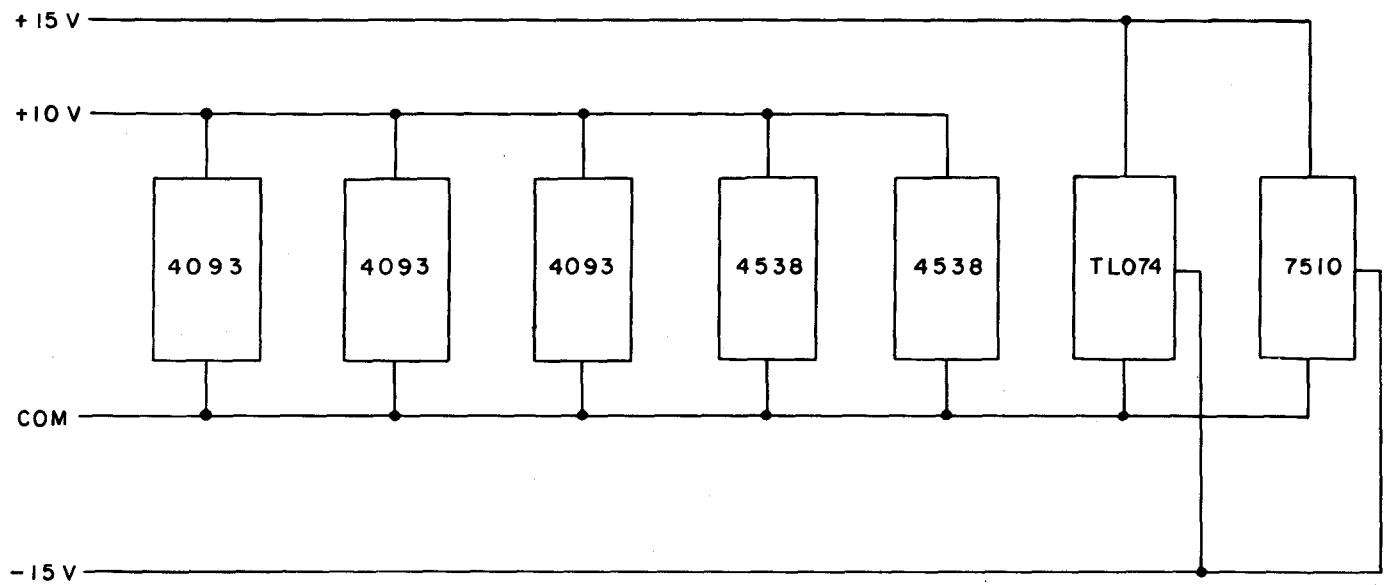

Figure 4.–Power distribution.

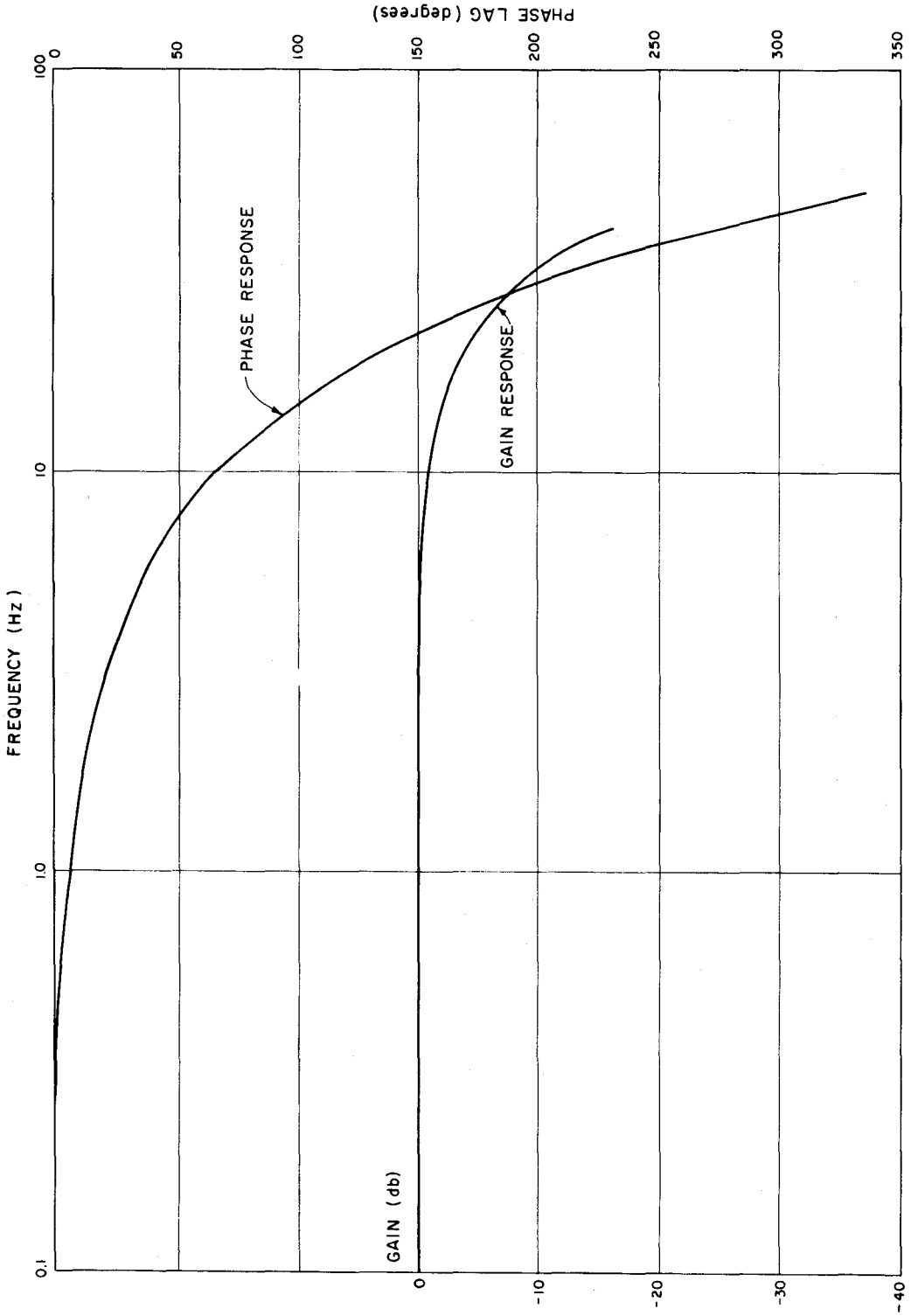

Figure 5.-Gain and phase response.

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